Design for Manufacturability (DFM)
Design for Assembly (DFA)

SMTA

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Welcome!!!

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Joe Belmonte

- **Motorola Information System Group**

  Mansfield Massachusetts (MA), USA

  1978 to 1995

  Manger of Advanced Manufacturing Engineering

- **Speedline Technologies**

  (MPM, Camalot, Electrovert)

  Franklin MA, USA

  1995 to 2007

  Director of Applications Engineer and

  Principal Consultant

Joe Belmonte

- **Bose Corporation**

  Framingham MA, USA

  2007 to 2009

  Director of Advanced Manufacturing Engineering

- **ITM Consulting**

  Durham New Hampshire, USA

  2009 to Present

  Principal Consultant

Whatever comes out of these gates, we've got a better chance of survival if we work together. Do you understand? If we stay together, we survive.

Gladiator Movie Quotes by Author Unknown

Seminar Agenda

- Definition of DFM
- Customer Satisfaction Requirements
- Functional Responsibilities of DFM
- Concurrent Engineering
- Early Supplier Involvement
- Well Defined Development Process
- Defining a Process
- Six Sigma and Statistical Thinking
- Understanding and Controlling Process Variation

Seminar Agenda

- Inspection and Test Planning
- Process Characterization Concepts
- Stencil Design
- Evaluating Printed Circuit Board Designs
- Software

“The significant problems we face cannot be solved at the same level of thinking we were at when we created them”

-- Albert Einstein

“We are what we repeatedly do.
Excellence, then,
is not an act, but a habit.”
-- Aristotle

Ultimate Purpose of DFM/DFA is Customer Satisfaction!!!!!

- Quality
- Reliability
- Cost
- Delivery
- Features

Design for Manufacturability

- Design for Manufacturability must include a detailed understanding of the processes that will be used to build the product, how the processes are developed, how the processes are controlled, and how continuous improvement is accomplished.

DFM&DFA Guidelines

The two most important “documents” the electronic assembler should have are:

- Workmanship Standards
- **Design for Manufacturability and Assembly (DFMA) Guidelines**

Design for Manufacturability Definitions

Design for Manufacturability

Design for Manufacturability is the process by which every aspect of the product and process design is formally evaluated to insure the lowest possible product cost, the fastest possible process cycle time, and the highest possible first pass yield.

Design for Manufacturability

> “Designing a product to be produced in the most efficient manner possible (in terms of cost, resources, and time) taking into consideration how the product will be processed, utilizing the existing skill base (and avoiding the learning curve) to achieve the highest yields possible”
>
> Phil Zarrow

Design for Manufacturability

Design for Manufacturability is the method for creating robust product designs that will be insensitive to long-term dynamic variation in the processes and materials used in the manufacturing and will be immune to foreseeable misuse of the product in the environment in which it is used. -- Motorola

DFM is the process whereby manufacturing and test engineers influence the product design to make it as manufacturable and testable as possible by minimizing cycle time, reducing parts, using standard processes and maximizing test coverage. -- Dave Reed, 3COM

What is DFM&DFA ?

- **Design for Assembly (DFA)** - is a technique which will minimize total product cost by targeting: *(this is the process side of product transformation process)*
    - Parts Count *(This is the major cost driver in Mfg.)*
    - Assembly Time
    - Part Cost
    - The Assembly Process

- **Design for Manufacturing (DFM)** - is a technique for minimizing fabricated part cost: *(this is the material and tooling side of the product development process*)
    - Optimizing the Fabrication Process
    - Material Selection
    - Part Cost
    - Tooling Strategies to reduce cost
    - Tooling Cost Estimates

Customer Satisfaction Requirements

Customer Satisfaction Requirements

- A customer has a right to expect the product to be delivered without defects
  - A defect is any variation of a required characteristic of the product or its parts, which is far enough removed from its target value to prevent the product from fulfilling the physical and functional requirements of the customer

Customer Satisfaction Requirements

- A customer has a right to expect the product to be delivered when promised
  - Every occurrence of a defect within the manufacturing process requires time to analyze, repair, and test.

Customer Satisfaction Requirements

- A customer has a right to expect the product not to experience early life failure
  - Early life failures are the result of latent defects, or abnormalities, which will cause failure at some future time, depending on the degree of abnormality and amount of applied stress. Latent defects are not detectable by normal test or inspections.

Customer Satisfaction Requirements

- A customer has a right to expect the product not to fail excessively in service
  - If the product design is robust, it will be insensitive to long-term dynamic variation in the process and materials used in manufacturing and will be immune to foreseeable misuse of the product in the environment in which it is used.

Customer Satisfaction Requirements

- Delivered defects are directly proportional to the total number of defects found in the entire manufacturing process.
- Average cycle time per unit is directly proportional to the total number of defects per unit.
- Latent defects are directly proportional to the total number of defects found in the entire manufacturing process.

Customer Satisfaction Requirements

- Reducing the total number of defects per unit in the entire manufacturing process will:
  - Reduce delivered defects
  - Reduce the cycle time per unit
  - Reduce early life failure rate

Customer Satisfaction Requirements

- Reduced total defects per unit will result in:
  - Increased customer satisfaction
  - Reduced warranty cost
  - Reduced manufacturing cost

Functional Responsibilities of DFM

Functional Responsibilities:

Development Engineering (Product Design)

- Using supplied capability studies for suppliers and internal processes, design for 6 sigma performance for both supplier and internal processes
- Set supplier piece part specifications at 4.5 sigma based on supplier capabilities.
- Calculate sub-assembly tolerances statistically, then check the prototypes against the calculations. When changes are made in components, maintain up-to-date assembly output calculations.
  - Supply calculations to assist in new product start ups
  - Manufacturing provides performance data to development for use in next product design

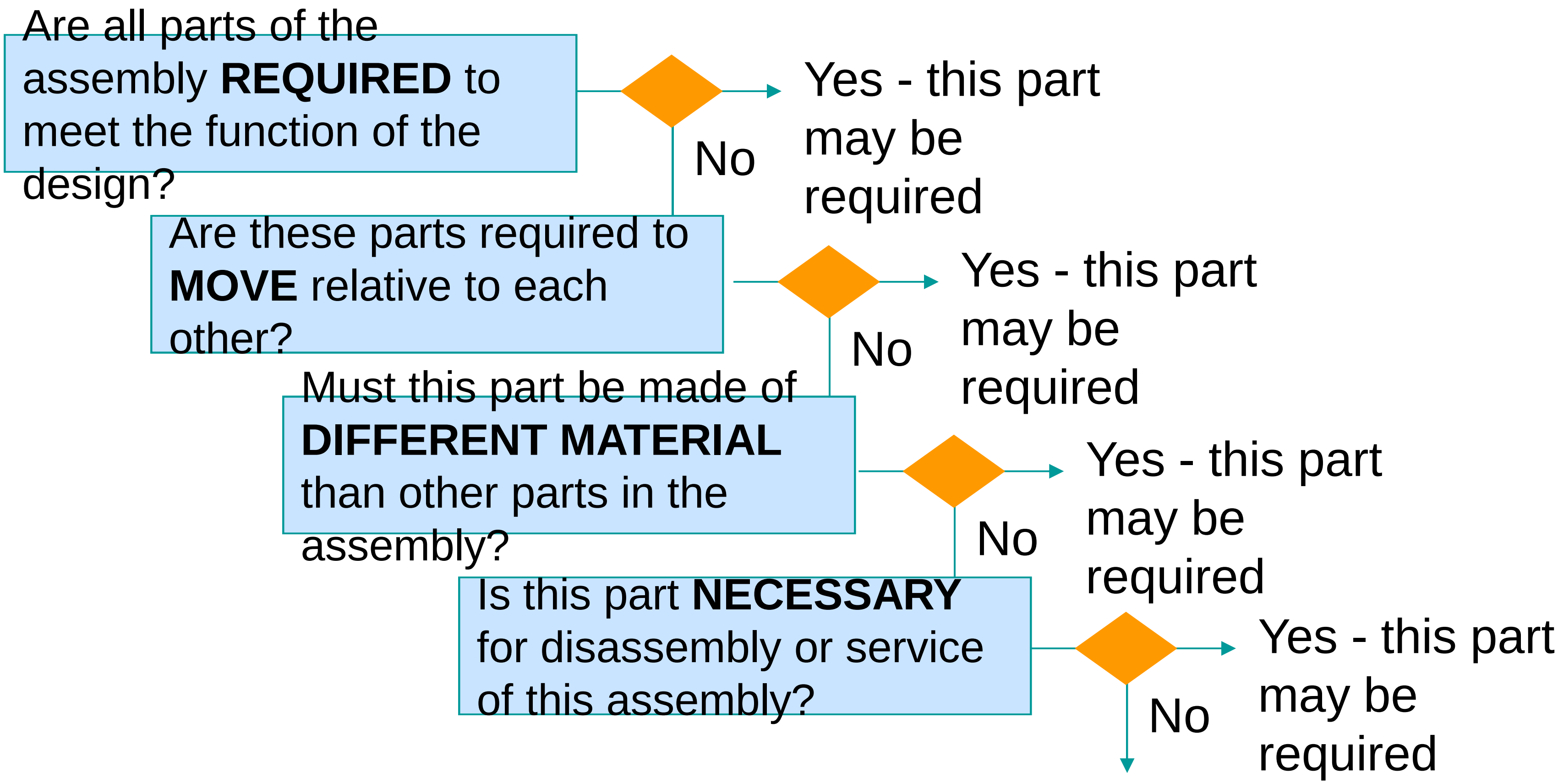
Design for Assembly DFA

Reduced part count is the MAJOR advantage to practicing design for assembly DFA

Part count drives/touches every aspect of an organization

Design for Assembly DFA

Unnecessary Parts Test



Are all parts of the assembly **REQUIRED** to meet the function of the design?

Yes - this part may be required

No

Are these parts required to **MOVE** relative to each other?

Yes - this part may be required

No

Must this part be made of **DIFFERENT MATERIAL** than other parts in the assembly?

Yes - this part may be required

No

Is this part **NECESSARY** for disassembly or service of this assembly?

Yes - this part may be required

No

Part is a candidate for elimination

Building better products requires a good comparative perspective about other companies to gain insight into other sources of outstanding performance

Product Development Performance
Kim Clark & Takahiro Fujimoto

Definitions

- **Benchmarking**
  - Is the continuous process of measuring products, services and practices against the toughest competitors or those recognized as industry leaders.
- **Competitive Intelligence**
  - Is the process of gleaming and combining disparate information about a competitor in order to deduce its objectives.
- **Reverse Engineering**
  - Is the systematic dismantling of a product to understand its technology with the purpose of replication.

COMPETITIVE COMPARISON

Professional Fixed Base Routers

FEATURES	MILWAUKEE 5615-20	PORTER CABLE 690	DEWALT 610	BOSCH 1617	BOSCH 1617EVS	MAKITA RF1100	MAKITA RF1101
Maximum HP	1-3/4	1-1/2	1-1/2	1-3/4	2	2-1/4	2-1/4
Amps	11.0	10.0	9.0	11.0	12.0	11.0	11.0
No-Load Speed (RPM)	24,000	23,000	25,000	25,000	8,000 - 25,000	24,000	8,000 - 24,000
Weight (lbs)	8.75	8.00	7.30	7.50	7.70	7.10	7.10
Tactile BodyGrip w/Hand Strap	YES	NO	NO	NO	NO	NO	NO
Tactile Palm-Grip Side Handles	YES	NO	NO	NO	NO	NO	NO
Motor Locking Mechanism	Lever	Wingnut	Wingnut	Lever	Lever	Lever	Lever
Collet Bit Shank Capacity	1/4, 1/2	1/4, 1/2	1/4, 1/2	1/4, 1/2, 3/8	1/4, 1/2, 3/8	1/4, 1/2	1/4, 1/2
Collet Type	2 Piece-Self Releasing	3 Piece-Self Releasing	2 Piece-Non Self Releasing	3 Piece-Self Releasing	3 Piece-Self Releasing	3 Piece-Self Releasing	3 Piece-Self Releasing
Collet Length/Collet Segments	1-1/8" / 8 Seg.	1-1/8" / 4 Seg.	7/10" / 1 Seg.	1" / 8 Seg.	1" / 8 Seg.	1-1/8" / 4 Seg.	1-1/8" / 4 Seg.
Collet Wrenches	Forged (1-1/8")	Stamped (1-1/8")	Stamped (3/4", 1")	Forged (16mm,24mm)	Forged (16mm,24mm)	Stamped (1-1/8")	Stamped (1-1/8")
Cord Length (ft)	8	7	8	10	10	8	8
Sub-base Diameter	6	5-3/4	6	6	6	5-3/4	5-3/4
Sub-base Center Hole Diameter	2-1/2	1-3/16	1-1/8	2-1/16	2-1/16	1-3/16	1-3/16
Depth Adjustment System	Linear (Macro/Micro)	Helical (Micro)	Linear R&P (Micro)	Linear (Macro/Micro)	Linear (Macro/Micro)	Helical (Micro)	Helical (Micro)
Above the Table Depth Access	YES	NO	NO	NO	NO	NO	NO
Switch Type/Location	Rocker - Body (Vert)	Toggle - Body (Horiz)	Toggle - Body (Horiz)	Rocker - Body (Horiz)	Rocker - Body (Horiz)	Toggle - Top	Toggle - Top
Constant Switch/Cord Location	YES	NO	YES	YES	YES	NO	NO
2001 List Price	$285	$290	$270	$307	$349	$337	$370
2001 Best Net Price	$128	$135	$122	$145	$166	$160	$176

Milwaukee

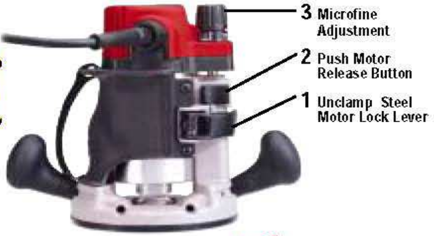
BodyGrip™ &
D-HANDLE ROUTERS

5615-20 & 5615-21
FEATURES
GET THE UPPER HAND

Constant Switch & Cord Position

3-Step

Fast, Accurate Linear Depth Adjustment*



3 Microfine Adjustment
2 Push Motor Release Button
1 Unclamp Steel Motor Lock Lever

*Patent Pending

Milwaukee

**BodyGrip™ &
D-HANDLE ROUTERS**

Boothroyd Dewhurst DFMA® Software Tools and Services

- Founded in 1985 in Wakefield Rhode Island USA
- Provides product design and product manufacturability software tools and consulting services

Functional Responsibilities:

Component Engineering

- At the time of component qualification, display in the component qualification report the actual data on each critical parameter. Show any corrective action required by the supplier so that all parties are aware of what must be done to finish qualification of the part to make it acceptable.
- Mechanical dimensions must be qualified to the same design margins as those of electrical parameters. This will be done when supplier data for the first piece parts is scrutinized.

Functional Responsibilities:

New Product Introduction Engineering

- Work as closely as possible, as early as possible, with the product development team to insure all aspects of manufacturability and testability are built into the product design from its inception. Work as a member of the product development team.
- Coordinate and communicate with all concerned groups (manufacturing, sustaining engineering, development, purchasing, component engineering, quality, marketing, sales, etc.) the product development status at each step of the process.

Functional Responsibilities:

Process/Manufacturing Engineering

- Perform process capability studies on all existing processes and place under statistical control. Supply current capability to product development engineers.
- Start a procedure of process improvement that brings performance of each process to six sigma levels. As processes improve, update development engineering on the new capabilities.

Functional Responsibilities:

Process/Manufacturing Engineering

- During the prototype and pilot runs, every failure must be treated as either a parametric or catastrophic failure, and its source must be corrected by design or process improvements. This applies both to internal failures and supplier failures.
- At prototype and pilot runs, and in conjunction with production personnel, re-check the process capability data to ensure nothing has changed. Maintain statistical control and statistically analyze for design margins to six sigma. Identify each failure and treat as described.

Functional Responsibilities:

Product Quality Engineering

- Perform specification compliance evaluations
- Perform accelerated life/reliability evaluations and statistical analysis on all critical parameters. Report the actual design margins found in the finished product to product design and manufacturing.

Functional Responsibilities:

Advanced Manufacturing Technology

- Calculate process capabilities (Cp/Cpk) on each new piece of equipment or new process before turning them over to manufacturing.
- The manufacturing engineer responsible for the new equipment or process will verify it in production mode and establish the capabilities and statistical controls (SPC) for ongoing manufacturing.

Functional Responsibilities:

Supplier Component Engineer and Purchasing

- Develop supplier process capabilities and furnish them to development engineering.
- Work with suppliers to improve process capabilities when the design cannot tolerate variation in the supplier’s existing processes.
- Ensure supplier compliance to SPC requirements and require that proof of control is supplied with each lot of material.

Concurrent Engineering

New Product Development Process

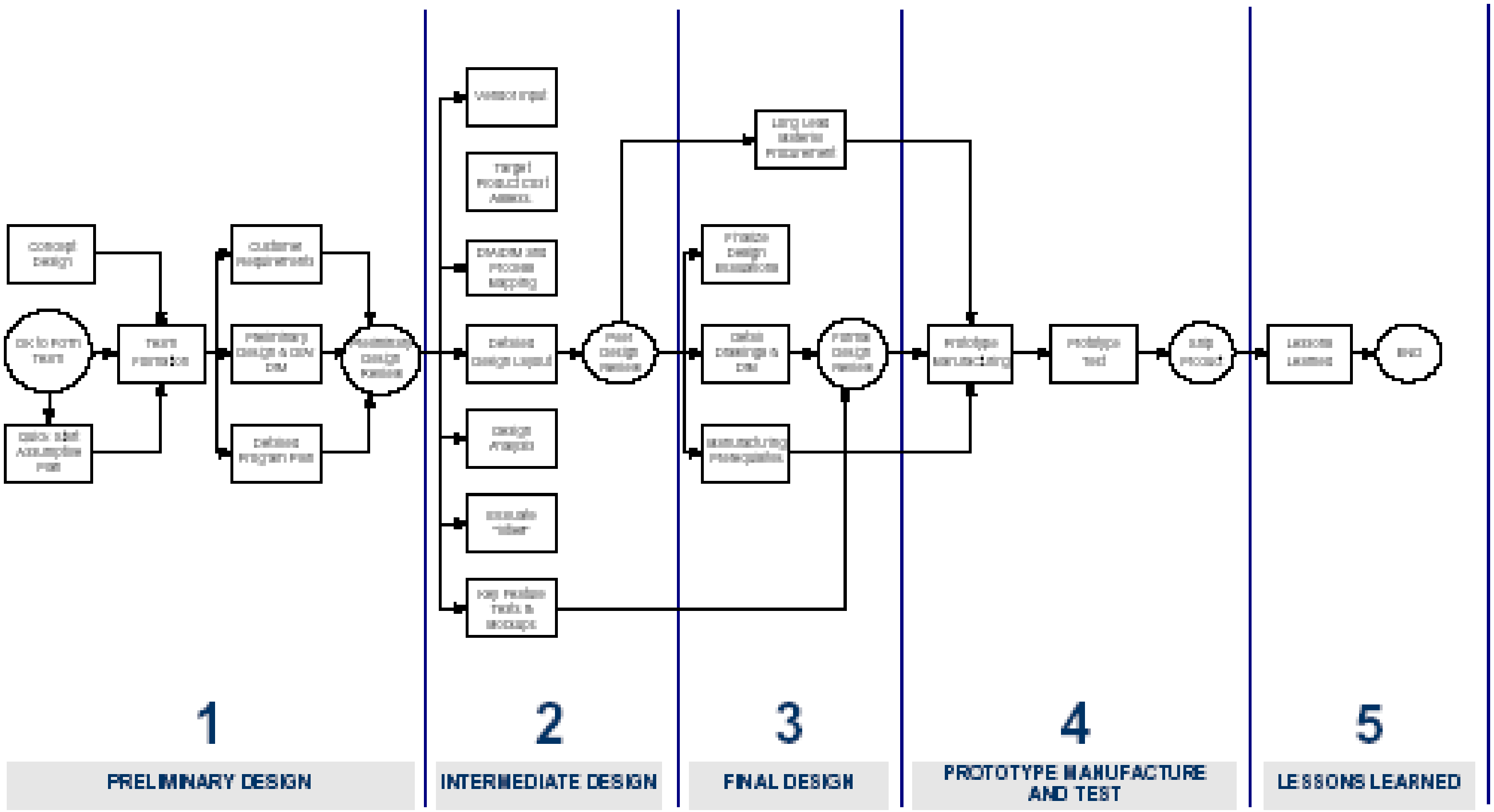
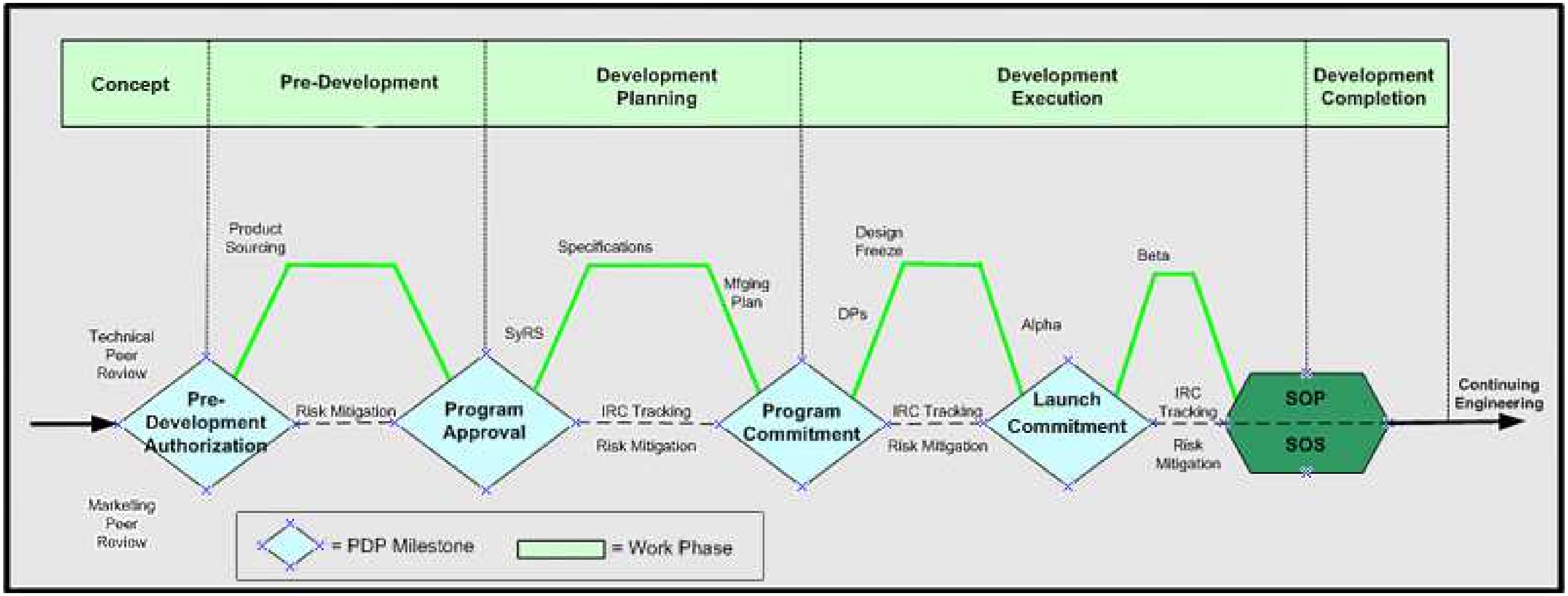


Figure 3-1 New Product Development Process (NPDP) Schedule — High Level

Product Development Process



DFMA process and tools can be applied throughout the product development cycle

The Cost of Making Changes

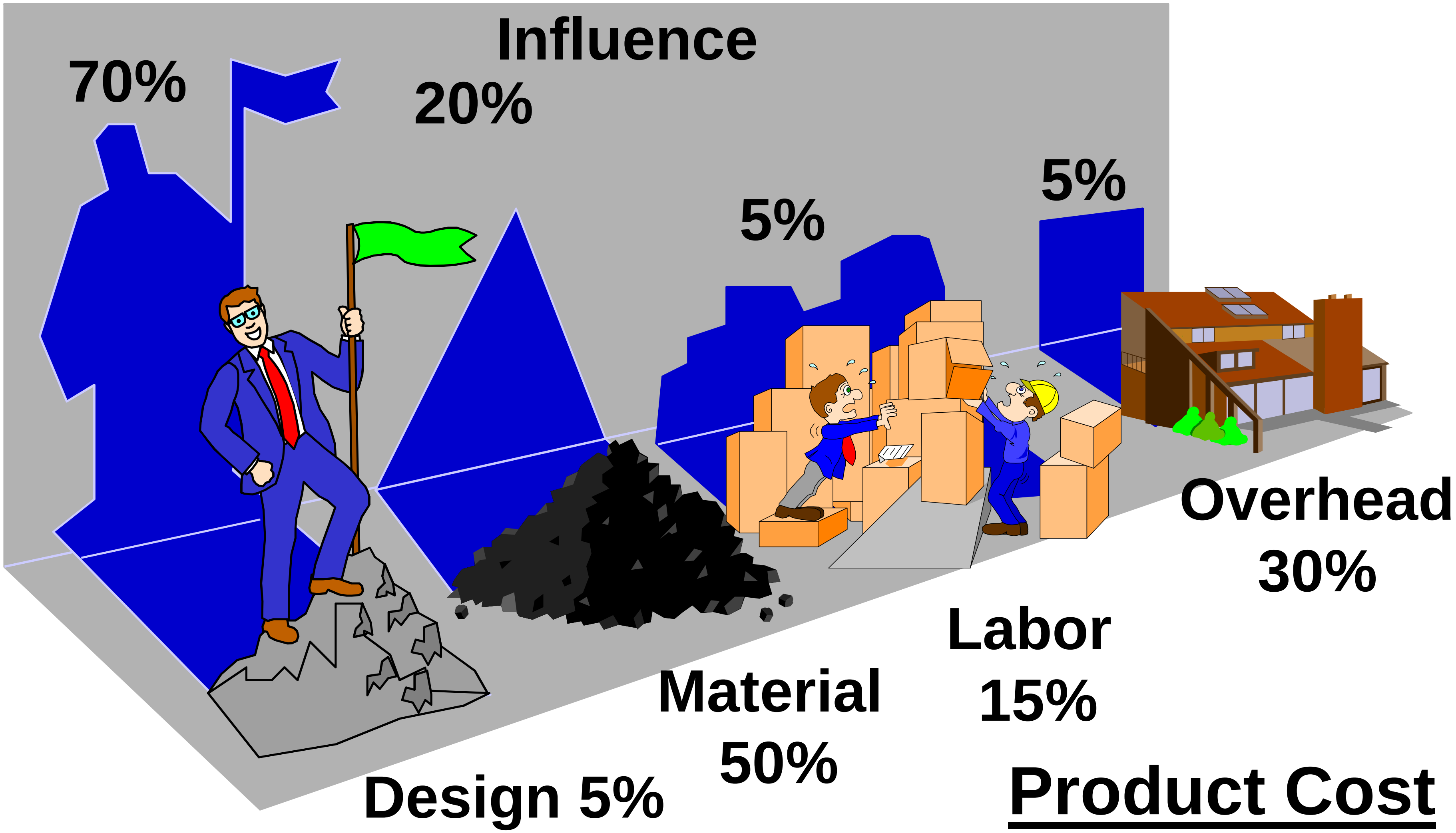
According to President Hiroshi Hamada, Ricoh did not detect a problem with one of its copiers until the machines were shipped to customers.
Had the problem been corrected earlier, before the start of production, he estimated the cost of correcting the problem at various stages as follows:

At the design phase:	**$ 35**
Before procuring parts:	**$177**
Before start of production:	**$368**

Instead, the cost of correcting this problem was:

$590,000.00

Who Casts the Biggest Shadow?



Influence

70%

20%

5%

5%

Design 5%

Material 50%

Labor 15%

Overhead 30%

Product Cost

Adapted from Ford Motor Co.

Design for Manufacturability

75 to 90% of project/product costs

are determined during the first

7 to 8% of development time.

-- Paul Collins Ph.D., University of Washington and Strategy Research Applications

Concurrent Engineering

- Concurrent Engineering is a competitive strategy attempting to simultaneously achieve a portfolio of benefits in time, money, and novelty (features).
- Concurrent Engineering involves multiple functions involved in decision-making on product design so that downstream issues such as manufacturability, marketability, serviceability, and total life cycle problems are anticipated at very early product design stages.

-- Paul Collins Ph.D. University of Washington and Strategy Research Applications

Concurrent Engineering

- Product Development Time Reductions:
  - 40% to 67%
- Product Development Costs reductions:
  - 16% to 46% for Telecommunications
  - 55% to 95% for Aerospace
- Engineering Rework Reductions:
  - 50% to 54%

-- Paul Collins Ph.D. University of Washington and Strategy Research Applications

Early Supplier Involvement

Early Supplier Involvement

- Capture the vendor’s know how and experience early.
- Share a commitment to the product by working together from the start.
- Optimize the part design to take advantage of the vendor’s capabilities and processes.
- Optimize the part design for ease of manufacture with input from the vendor on the emerging design.
- Set target cost for tooling and parts using cost models to support the products cost goals. Use this data to open communications with vendors.

Early Supplier Involvement

- “Our customers teach us to be good suppliers; perhaps our suppliers could teach us to be good customers.”
- “We realize that we are not taking full advantage of the benefits of supplier design expertise early enough in our design process. Many of our customers have enjoyed these benefits for years. They know the value of supplier-customer design teams.”
- “Suppliers can help design in quality from the beginning, and shorten the product development cycle time” -- Gary Tooker, Motorola

Early Supplier Involvement

- The early supplier involvement process requires the trust and openness to share critical information between the customer and chosen supplier.
- A supplier must be prepared with personal capable of responding to the customer’s requirements.

Early Supplier Involvement

- These questions should be asked:
  - Do you have a standard item that can be substituted?
  - What are the available manufacturing alternatives?
  - Can you suggest a material alternative?
  - Do you have any suggestions that would reduce processing?
  - Are there any product design alternatives that can be made to assist you?

Early Supplier Involvement

- These questions should be asked:
  - Can you evaluate cost versus precision?
  - Can you suggest procedures to detect and remedy deviations?
  - Does your company have the technical expertise available in a time frame appropriate to the customer requirements?
  - Do you have any further suggestions that might reduce lead time, simplify the part, and/or reduce cost?

Early Supplier Involvement

- What are ways to insure 100% usable purchased parts and materials?
  - Cpk equal to or greater than 1.5
  - Supplier specifications that reflect true critical values
  - The specs supplied by the customer must allow the supplier to use the most efficient manufacturing process.
  - Internal policies and procedures must conform to the above.

Benefits of Early Supplier Involvement

- Lower development and part cost
- Optimized manufacturability
- Improved part quality
- Improved delivery schedules
- Improved communications
- Optimized product design

Benefits of Early Supplier Involvement

- Minimized design changes
- Reduced product development time
- Optimized material selection
- Utilized supplier technology
- Standardized parts
- Calculated Six Sigma design

Well Defined Development Process

Well Defined Development Process

- Be documented, graphically and textually
  - Key terms are defined
  - Documentation is distributed to and understood by all involved parties
- Be detailed and specific enough to serve as a working development blueprint; yet flexible enough to accommodate products of varying complexity
- Minimize all opportunities for parallel development

Well Defined Development Process

- Define the items listed for each phase:
  - Required inputs and sources
  - Constituent steps and tasks
  - Per step/task, roles and responsibilities
  - Outputs, including documentation specifications
  - Phase entry and exit criteria
  - Necessary functional involvement
- Be enforced and monitored

Well Defined Development Process

- A formal review should occur at the end of each development phase in order to:
  - Detect problems (potential defects) as close as possible to their point of origin.
  - Track and document sources of error and defects.
  - Uncover errors, but NOT to fix them (during the review)
  - Confirm outputs that do not require improvements.
  - Make projects more manageable.

Characteristics of Formal Phase Reviews

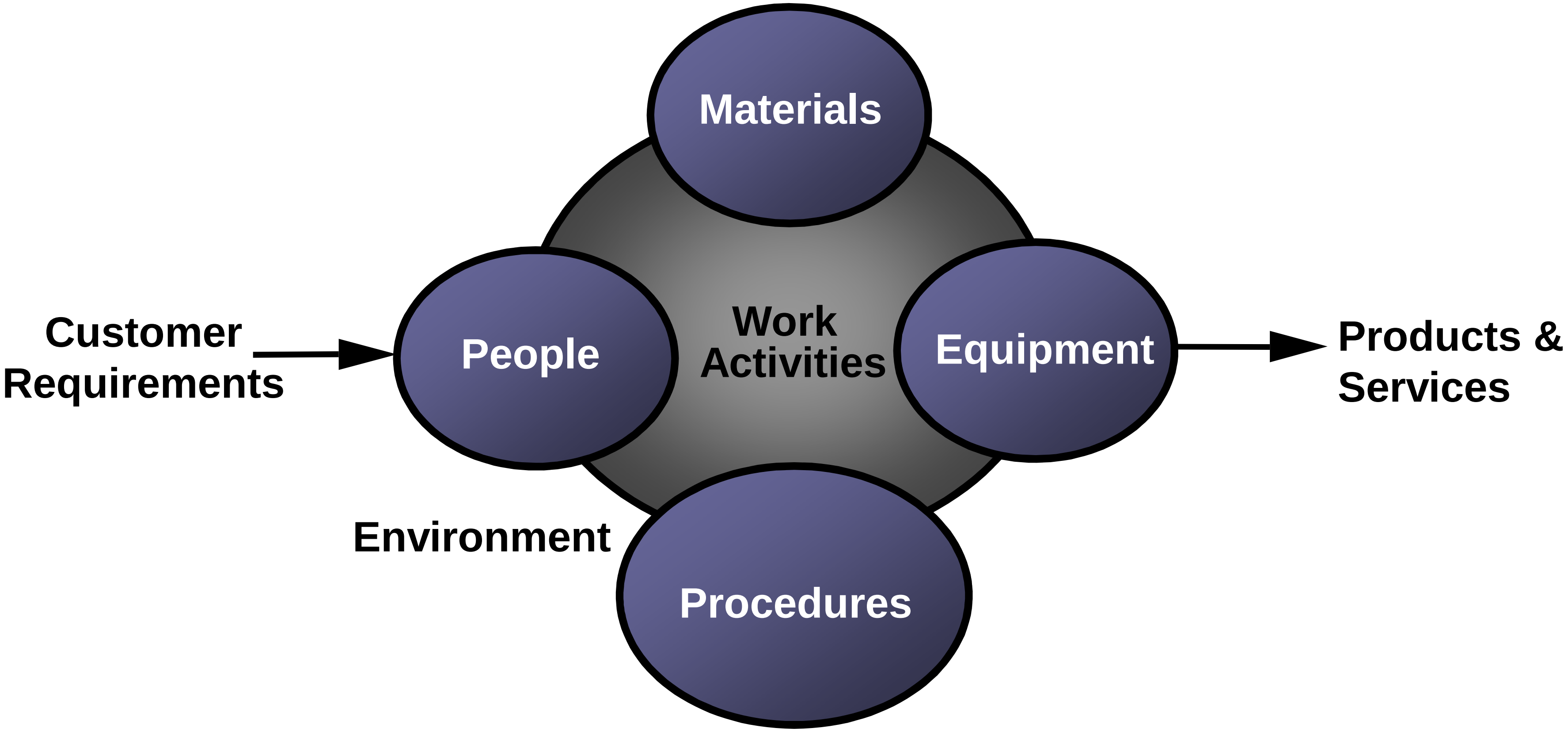
- Cross functional representation, including customers
- Material disseminated in advance
- Scope of material covers wide spectrum
- May need to occur over several meetings
- Coordinated by project leader
- Sign-off and follow-up report required

Defining a Process

Define the Process

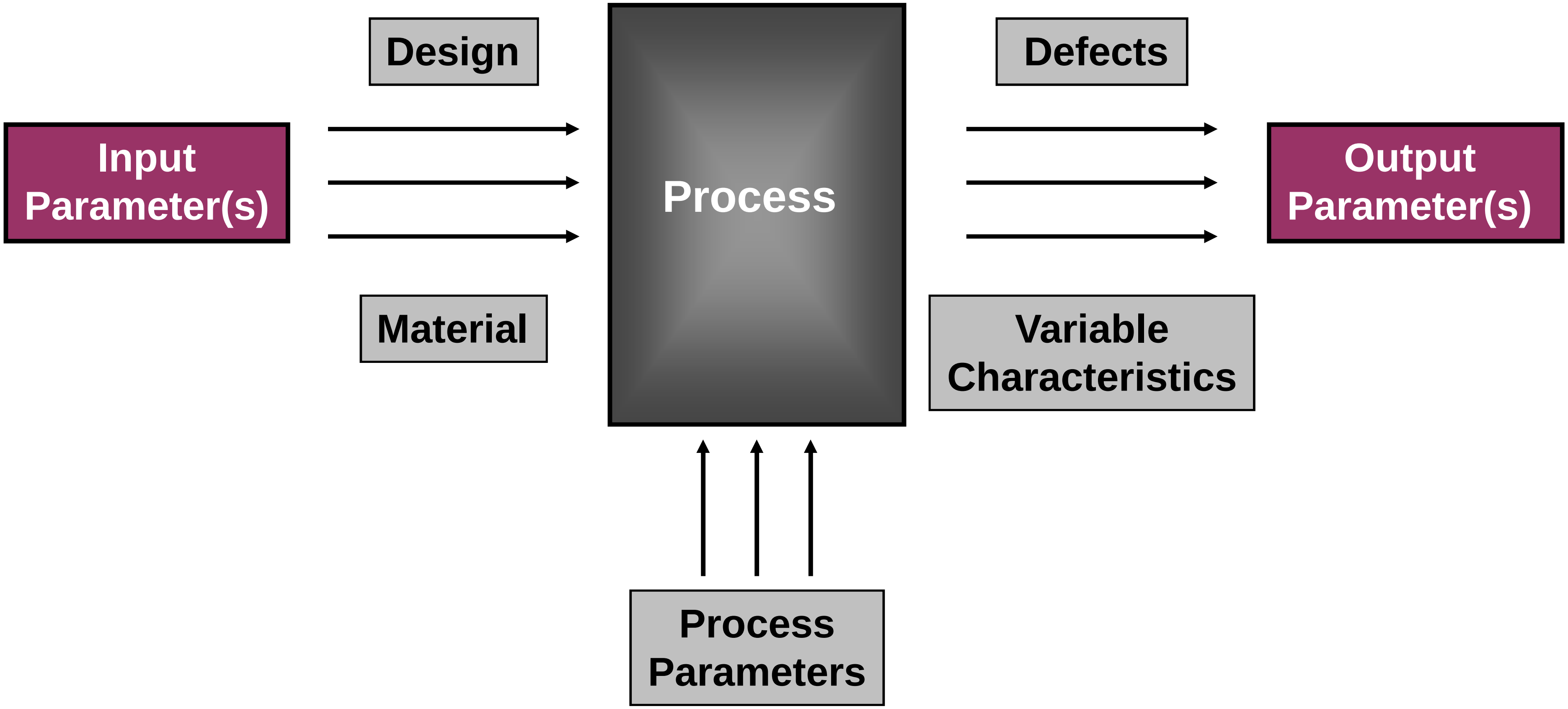
- The term “process” means different things to different people. So, it is important to clearly define what we mean by process.
- A process can be defined as the logical organization of people, materials, environment, equipment, and procedures into work activities designed to produce a specified end result.

Elements of a Process



A key/critical process is basically a "valued-added" process in the Macro Map which inhibits achieving 6 sigma quality in our products or services.

Defining Process Parameters



Design

Input Parameter(s)

Material

Process

Defects

Output Parameter(s)

Variable Characteristics

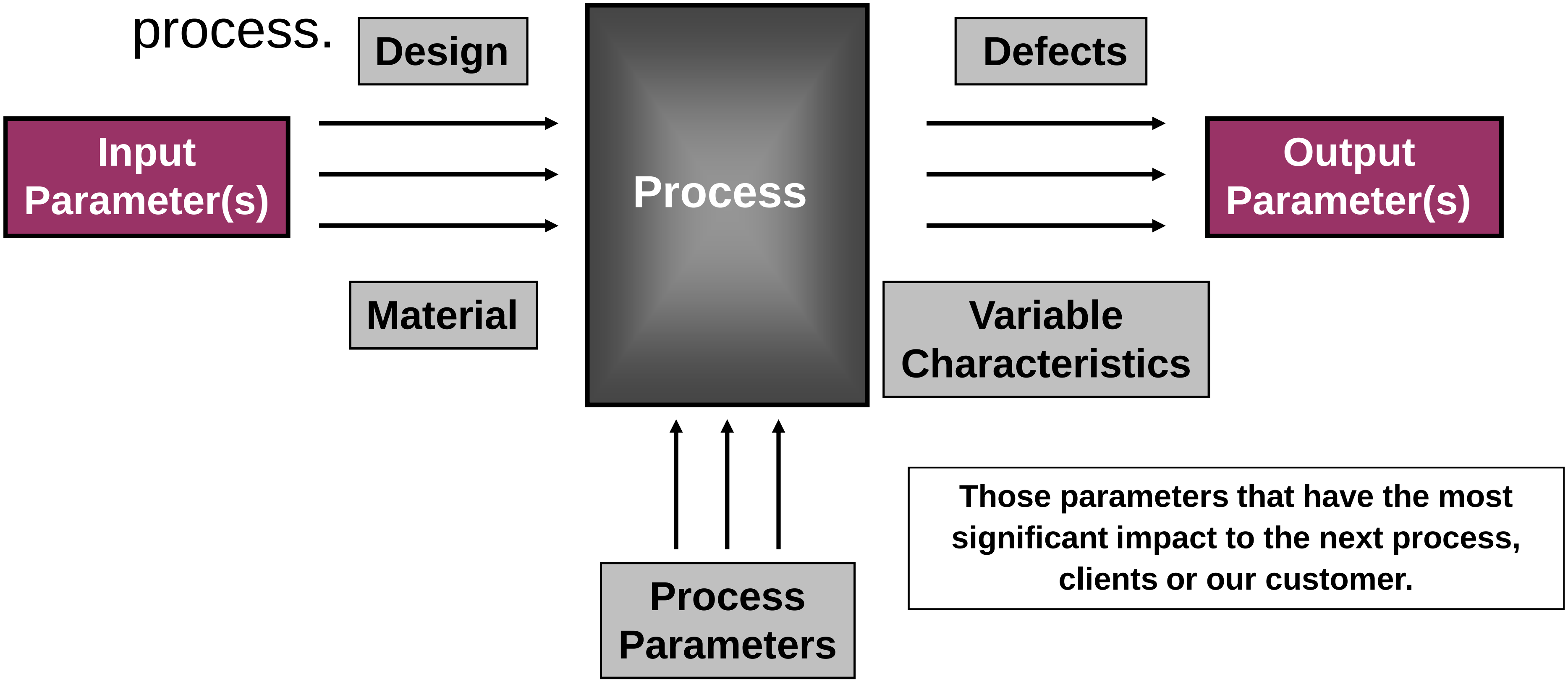
Process Parameters

Defining Process Parameters

- Input Parameters
  - A measurement system or a parameter in a process that is used in the creation of process output.
  - Input parameters are materials, methods, measurements, machines, people, and environment.
- Process Parameters
  - Steps or activities completed using the input parameters to generate a product or service.
- Output Parameters
  - The end result of a process. It may include as little as only one specific output on only one product or it my include as much as all products and all outputs produced by the machine(s) and/or operation(s) included in the process.

Identifying Parameters

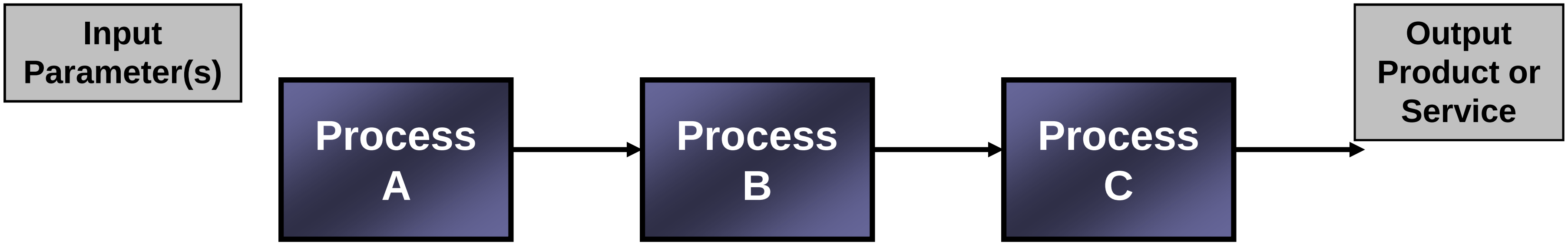
Choosing those parameters that will be the leading indicators to the quality level being produced by the process.



Those parameters that have the most significant impact to the next process, clients or our customer.

Process Mapping

- Understanding the flow of the process, all inputs, outputs, of each process steps.
  - Macro-Map : Macro-Mapping is the process of charting the coarse flow of an operation (such as a manufacturing line).
  - Micro-Map : Micro-Mapping breaks down a process in the Macro-Map into several consecutive sub-steps (identifying all inputs and outputs).



Input Parameter(s)

Process A

Process B

Process C

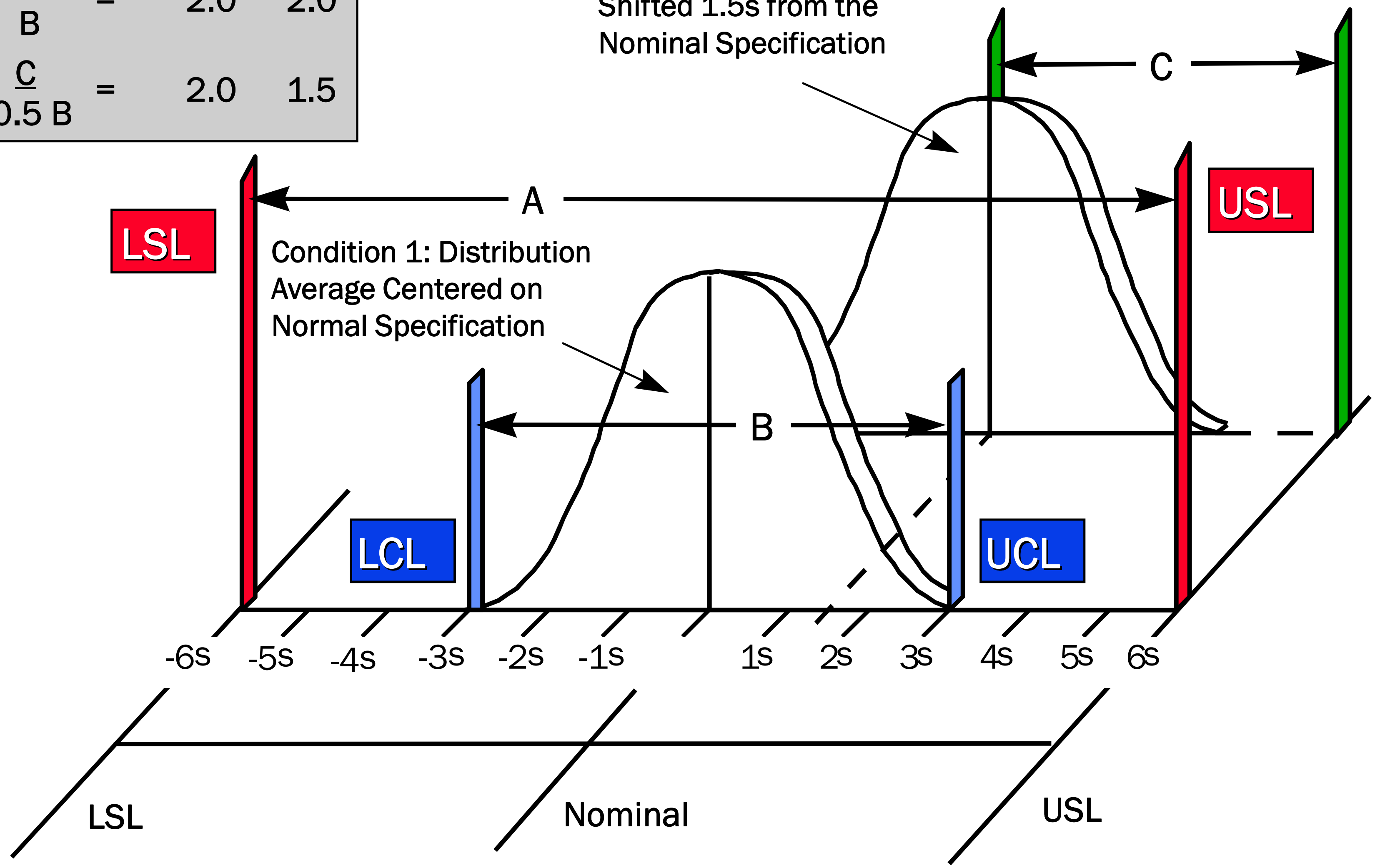
Output Product or Service

Methods Used to Identify Parameters

- Brainstorming Techniques
- Prioritization Matrix
- Cause and Effect Diagrams (Fishbone)
- Modified Cause and Effect Diagrams
- Weighted Voting
- Affinity Diagrams

Six Sigma
and
Statistical Thinking

Capability			Condition 1	Condition 2
C p =	$\frac{A}{B}$	=	2.0	2.0
C pk =	$\frac{C}{0.5\,B}$	=	2.0	1.5

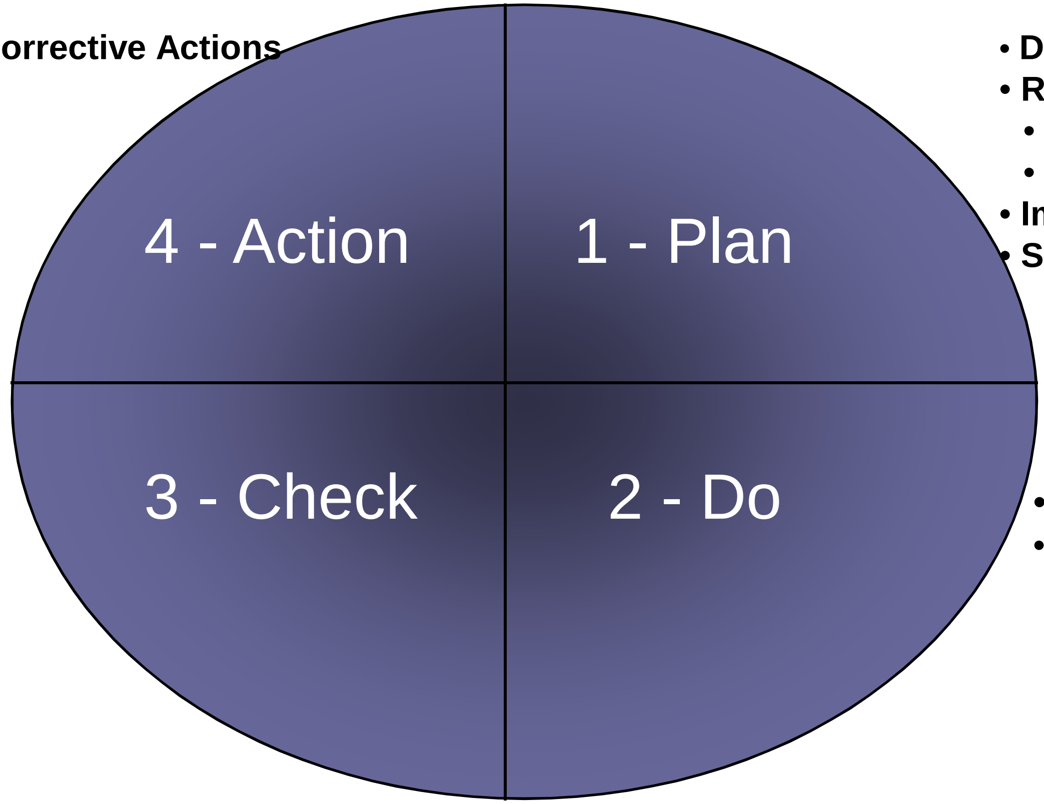


Condition 2: Distribution Average Shifted 1.5s from the Nominal Specification

Condition 1: Distribution Average Centered on Normal Specification

What is Six Sigma?

A discipline of continuous improvement to achieve Total Customer Satisfaction.



- Implement Permanent Corrective Actions
- Prevent Recurrence
- Control the Process
- Standardization
- Redesign

- Define Goals and Targets
- Recognize Parameters
  - Identify Key Opportunities
  - Identify Key Processes
- Improvement Plan
- Select Project/Team

- Measure Improvement
- Assess Effectiveness
- Review Projects

- Education and Training
- Implementation

Key Factors for Success

- **Management Leadership**
  - **Top down**
  - **Committed**
- Clear & Aggressive Goals
- Breakthrough Thinking
- Training (Black Belt Program)
- Reinforcing Successes
- Drive Six Sigma Quality through Statistical Thinking and Analytical Problem Solving

Six Sigma “Key Initiative” Challenges

- The achievement of “Error Free Performance” in Products, Processes and Services
  - Six Sigma Quality - 3.4 defects per million opportunities
  - Total Cycle Time Reduction - 10x improvement every 2 years
  - Six Sigma Designs
  - Process and Supplier Characterization
  - Variation Reduction in Processes and Designs
  - Cp/Cpk > 1.5
  - Total Customer Satisfaction
  - Software Quality - SEI
- Six Sigma is a highly disciplined and quantitative approach to improvements

Five Myths of Statistical Thinking & Analytical Problem Solving

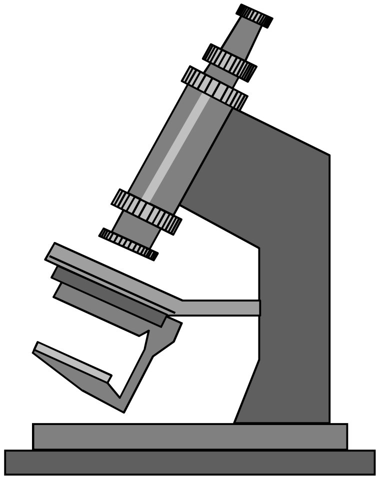
- Only works in manufacturing
- Is added effort, takes too long
- Requires large teams
- Creates a lot of bureaucracy
- Just another quality program

The Role of Continuous Improvement

- To achieve consistency in our processes, we need to reduce variation. But, how do we:
  - Measure the current levels of variation?
  - Decide what to work on next?
  - Know we have improved?
- To answer these questions, we must have a process and associated tools. It is here that statistics and statistical thinking play a major role.

The Role of Statistical Thinking in Continuous Improvement

- Statistics: The science of turning data into information for making business or engineering decisions in the presence of uncertainty. The electronics business is a data-driven industry. We apply statistical methods to enable us to make quantitative statements in the presence of variability.
- Statistical methods are like a microscope is to a scientist. They help us focus our expertise on the solution of the problem at hand.



Why Does Statistical Thinking Work?

- Creates Bottom Line Results ($)
- Uses a Disciplined Approach
- Managed by Data Approach
- Sound Statistical & Problem Solving Approach
- Creates Proficient Quality Professionals
- Standardized Approach that works Across Processes, Products and Organizations.

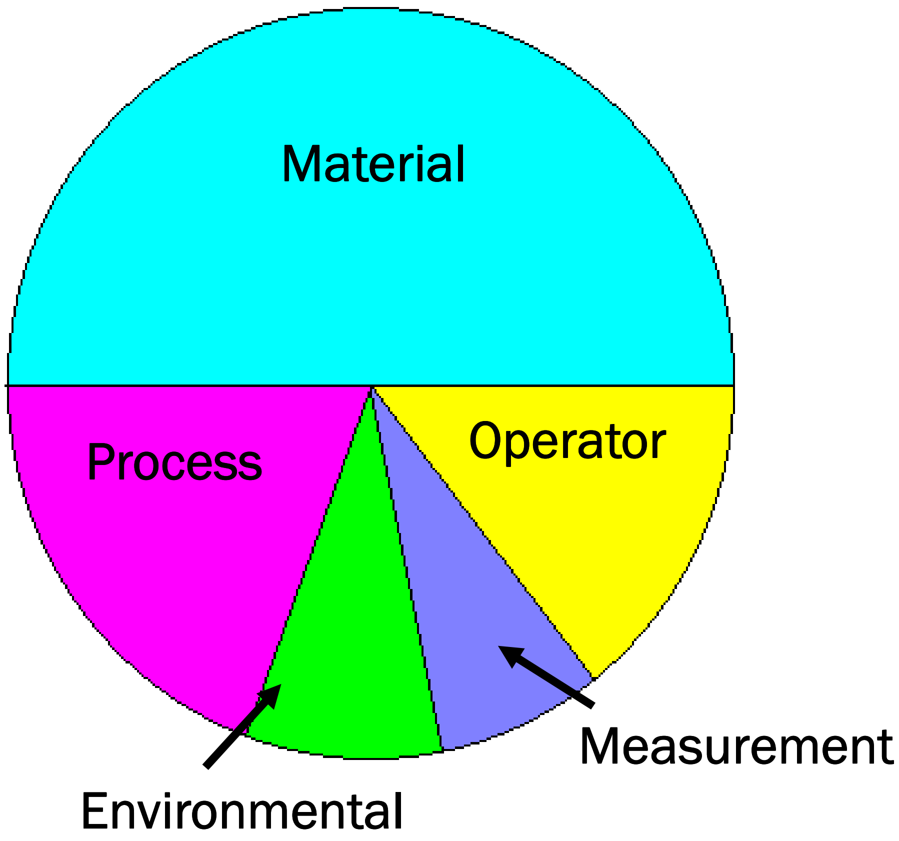
Statistical Thinking is Different and it Works

- Focused Approach
  - Phased Improvement Methodology
    - Define, Measure, Analyze, Improve and Control
  - Understanding and reducing variation are keys to success.
- Statistical Thinking is a way of thinking, a thought process, rather than a method of calculating.

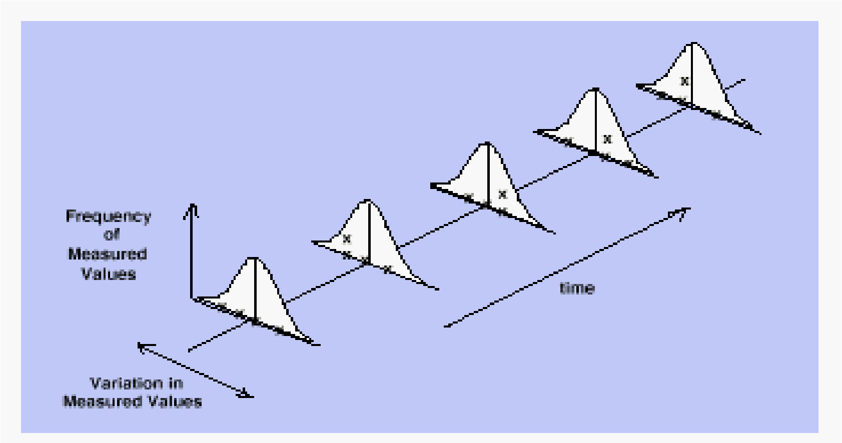
Process Variation

Components of Variation

In all aspects of the process…understand and control

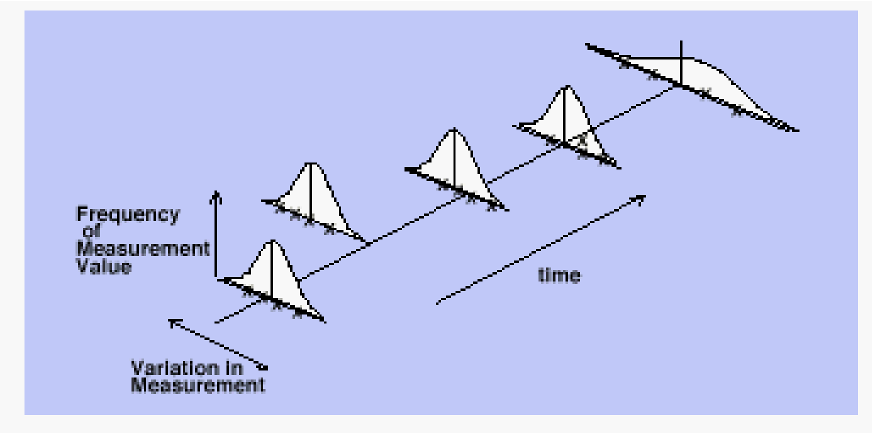


What Is Variation?



Common Cause

- Natural, expected variation
- Difficult to identify
- Cannot be eliminated
    - DOE can reduce
- Controllable
- Ex: Solder Paste Parameters, Temp, R/H, Lead Co-planar.

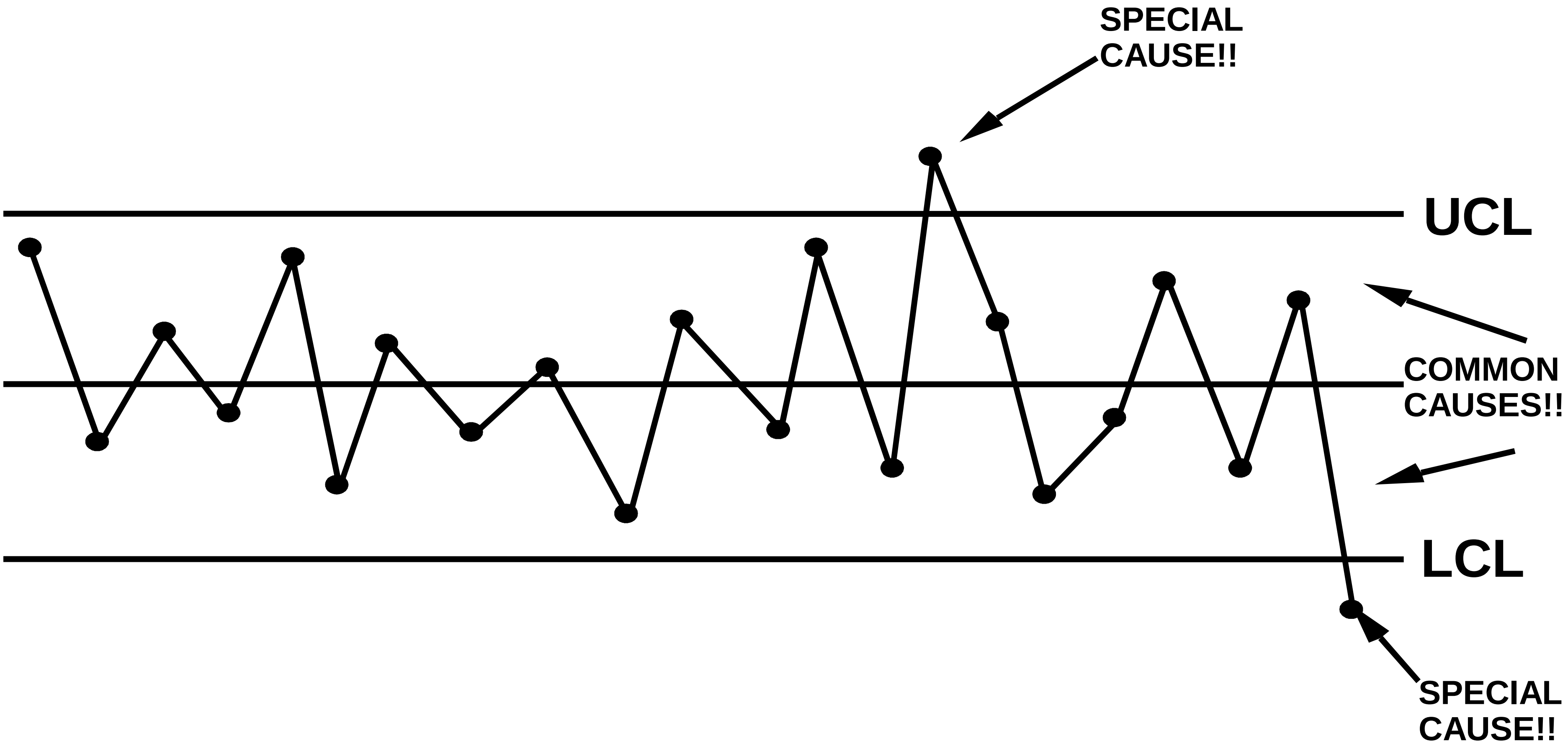


Special Cause

- Unnatural, not expected
- Easily Identified
- Can be eliminated
- Ex: Paste dried out on stencil, machine fail, setting changed w/o OK
- Never change operating parameters for special cause variation (do not tweak!!!)

Types of Defects

Special & Common Causes



Identification of Special and Common Causes

Corrective Action :

- SPC rule violations
  - "Special Cause" - changes, anomalies, unusual events
  - "Common Cause" - shift in mean, trend in mean, increased variability "
- Implement contaminate plan, and monitor for repeat occurrences.
  - -Stop defects from escaping to next process
  - -Keep process in operation while permanent corrective action is implemented
- For repeat occurrences tie specific cause to corrective action using problem solving methods.

Never change operating parameters for Special Cause Variations

Process “Tweaking”

The definition that best describes tweaking in the electronics manufacturing industry is:

  - “To touch something up, fiddle with the finishing touches or make tiny little changes. In our industry, tweak is usually used in sentences such as “I just have to tweak a little bit here and there and it will be perfect.“
  - That usually leads to a statement such as "I just tweaked this and THIS AND THIS AND THIS and this and OH NO now this...“

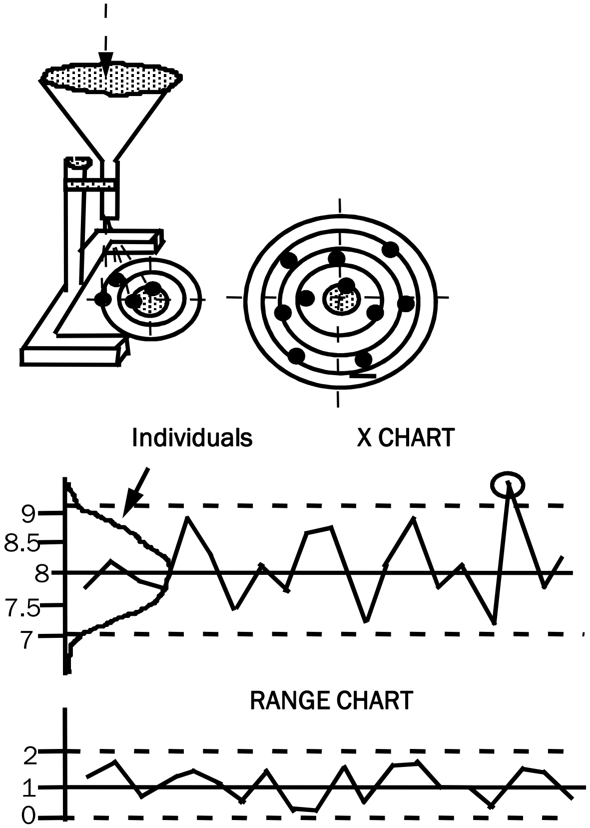
- If we have done our formal process development and optimization, we are monitoring the process using statistical process control (SPC), and understand the concepts of common cause and special cause variation, we should be adamant about **NEVER tweaking the process.**

Process “Tweaking”

- “What operating parameters should I allow my operators to adjust?”
  - NONE!!!!
- “But my operators are very well trained and have all worked with the process for many years. “With their knowledge and experience shouldn’t they be given the authority to change operating parameters to optimize performance?”
  - “NO”
- No process operator, no matter how knowledgeable or how experienced, should ever be allowed to adjust ANY operating parameter under ANY circumstances.

The Funnel Experiment

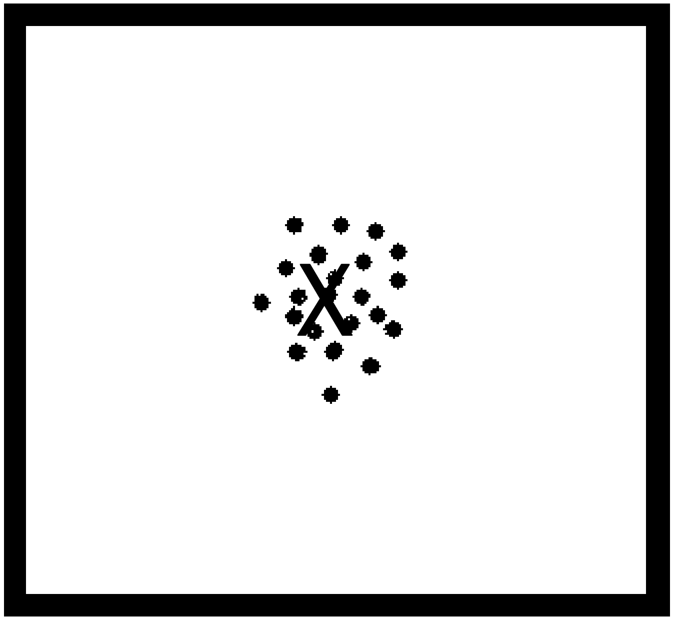
- The variation of a process reacts to adjustments made to improve the process.
- Dr. Deming discusses 4 different methods that have been commonly used to adjust processes.



Showing the spread of individuals on and Xbar and R chart.

Rule 1

- **Leave the funnel fixed, aimed at the target, no adjustment.**
- **Results: this is by far the best choice. Rule 1 will produce a stable distribution of points. It produces minimum variance on any diameter drawn through the target**

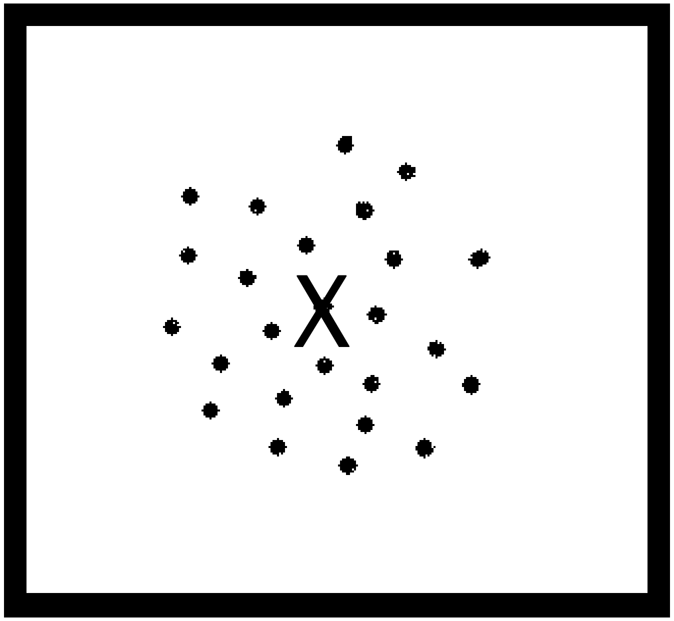


Rule 1

Rule 2

- **Adjust for the error by moving the target the error distance in the opposite direction of its last position.**

- **Tweaking! Never do it. Produces a stable process, but higher variance than rule 1.**

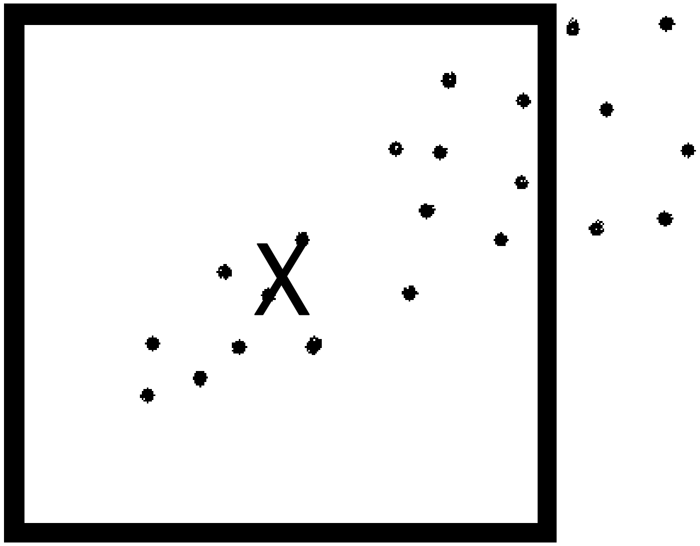


Rule 2

Rule 3

- Adjust for the error by moving the target the error distance in the opposite direction of the target

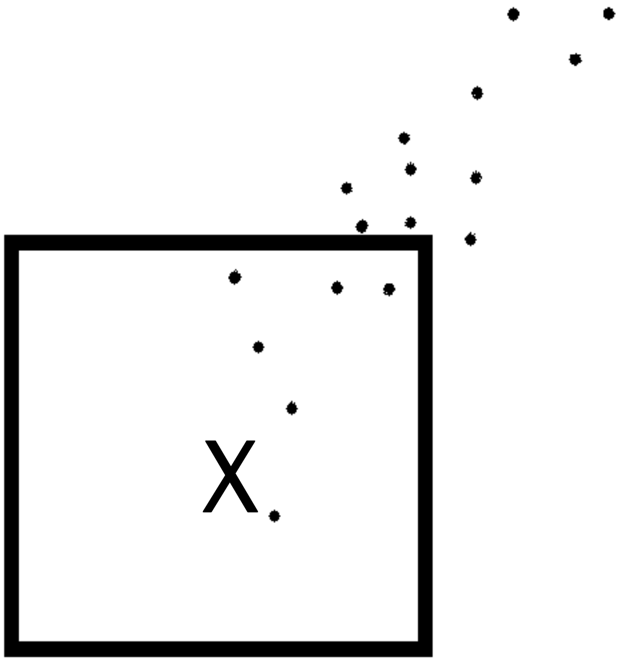
- Worse than tweaking explodes.



Rule 3

Rule 4

- **Set the funnel at each drop right over where it last hit.**
- **Explodes**

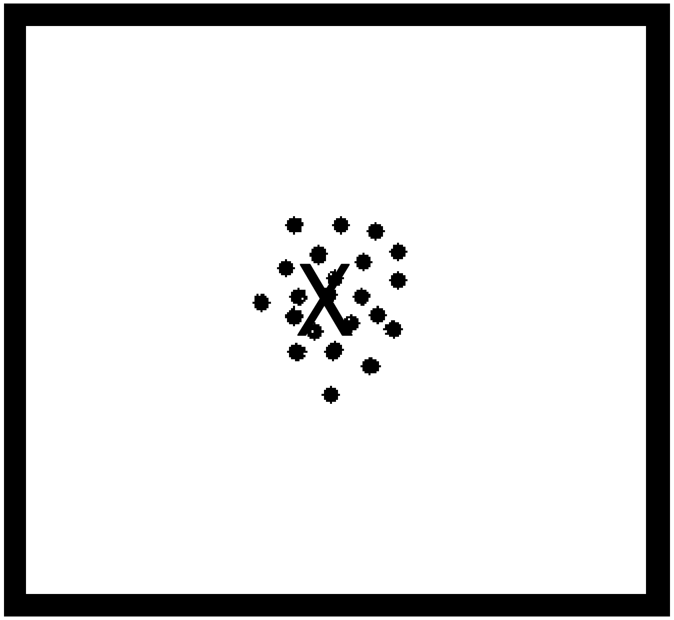


Rule 4

Relate to Traveling to Work: Goal 7:00 AM Arrival

Rule 1: Choose a reasonable route and consistently follow the route leaving your home at the same time each day.

Day	Departure	Arrival
1	6:30 a.m.	7:05 a.m.
2	6:30 a.m.	6:58 a.m.
3	6:30 a.m.	6:55 a.m.
4	6:30 a.m.	7:00 a.m.
5	6:30 a.m.	7:02 a.m.

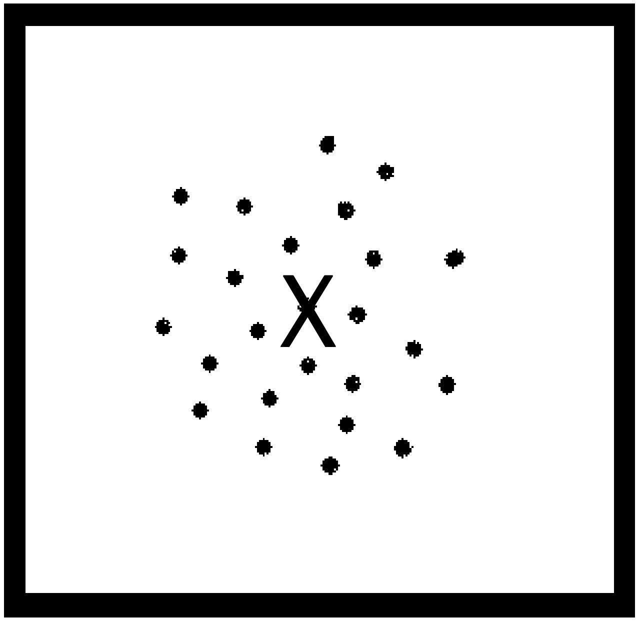


Rule 1

Rule 2

Compensate the amount of time you arrived at work early or late by leaving your home that much earlier or later, and continue adjusting you’re departure each day based on the previous day’s departure.

Day	Departure	Arrival
1	6:30 a.m.	7:05 a.m.
2	6:25 a.m.	6:50 a.m.
3	6:35 a.m.	7:15 a.m.
4	6:20 a.m.	7:00 a.m.
5	6:20 a.m.	6:50 a.m.

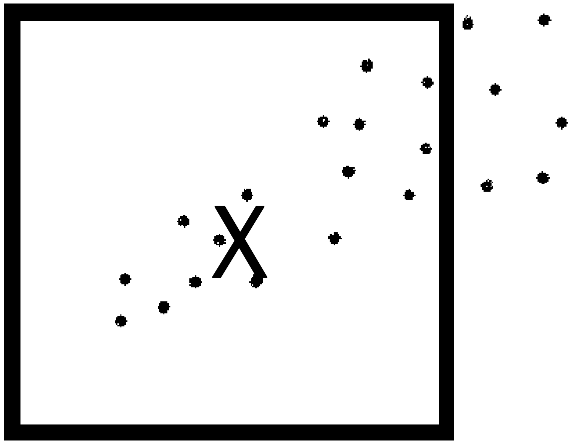


Rule 2

Rule 3

Compensate the amount of time you arrived at work early or late by leaving your home that much earlier or later than the original departure time, and continue adjusting your original departure time each day based on how early or late you were the previous day.

Day	Departure	Arrival
1	6:30 a.m.	7:05 a.m.
2	6:25 a.m.	6:50 a.m.
3	6:40 a.m.	7:15 a.m.
4	6:15 a.m.	6:40 a.m.
5	6:50 a.m.	7:25 a.m.

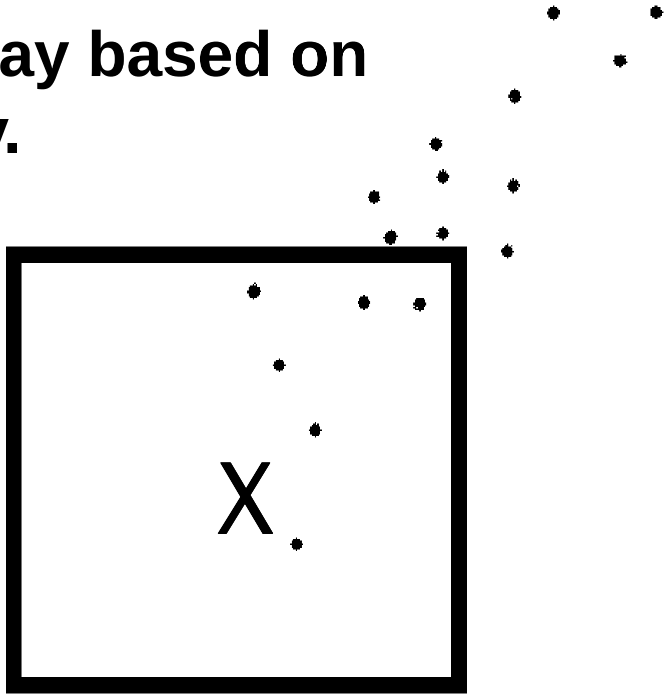


Rule 3

Rule 4

Compensate the amount of time you arrived at work early or late by leaving your home at the previous days arrival time, and continue adjusting your departure time each day based on the time you arrived the previous day.

Day	Departure	Arrival
1	6:30 a.m.	7:05 a.m.
2	7:05 a.m.	7:30 a.m.
3	7:30 a.m.	8:15 a.m.
4	8:15 a.m.	8:45 a.m.
5	8:45 a.m.	9:20 a.m.



Rule 4

What Process Performance Metric is Important

- The bottom line — the only metric that measures how well a process line is performing — is how many good products are built each day.
  - How many of what we build today can we ship to our customers?

- Good product is one built in an acceptable time that passes all required testing the first time **without any** inspection, touch-up, or repair.

Cycle Time/Throughput Balance

- There is a definite balance between product cycle time (how long it takes a product to get from beginning to end of the manufacturing process) and the quality of that product.
- Producing defective product just to achieve some required cycle time is certainly not acceptable; nor is slowing the process unduly to minimize every possible defect.
- We must understand and optimize this balance.

Inspection
and
Test
Planning

Inspection & Test Planning

- All inspection and test processes are NON VALUE ADDED functions.
- Inspection and test processes should be kept to a minimum.
- Focus on capable, stable processes to produce products that will minimizes the requirement for inspection and test.

Inspection & Test Planning

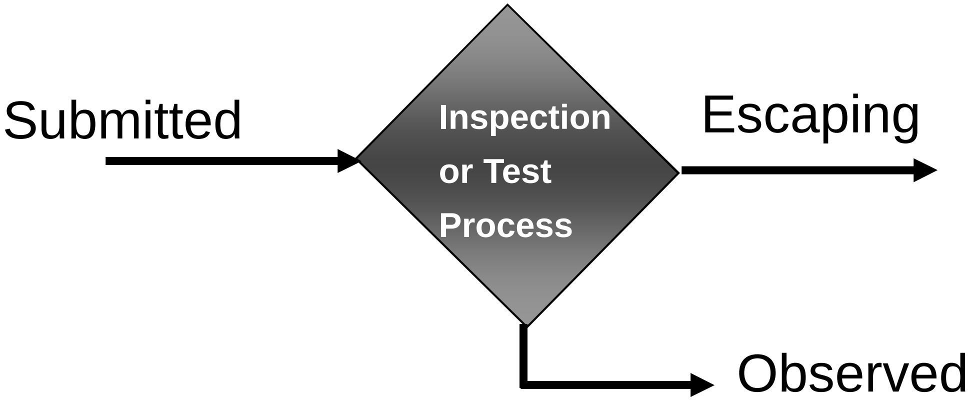
- Inspection and test planning is the activity of:
  - Designating the stations at which inspection or test should be performed.
  - Establishing the effectiveness of each inspection and test process.
  - Identifying which process contributes the most defects.

Inspection & Test Planning

- How can Inspection & Test Planning assist in Quality Planning ?
- Knowing the observed defect level, inspection and test effectiveness, we can estimate the submitted defects and escaping defects.

Inspection & Test Planning

- For example:
  - Observed Defects = 0.25 dpu
  - Insp. Or Test Effectiveness = 0.8
  - Submitted Defects = 0.31 dpu (0.25/.8)
  - Escaping Defects = 0.06 dpu (0.31 - 0.25)



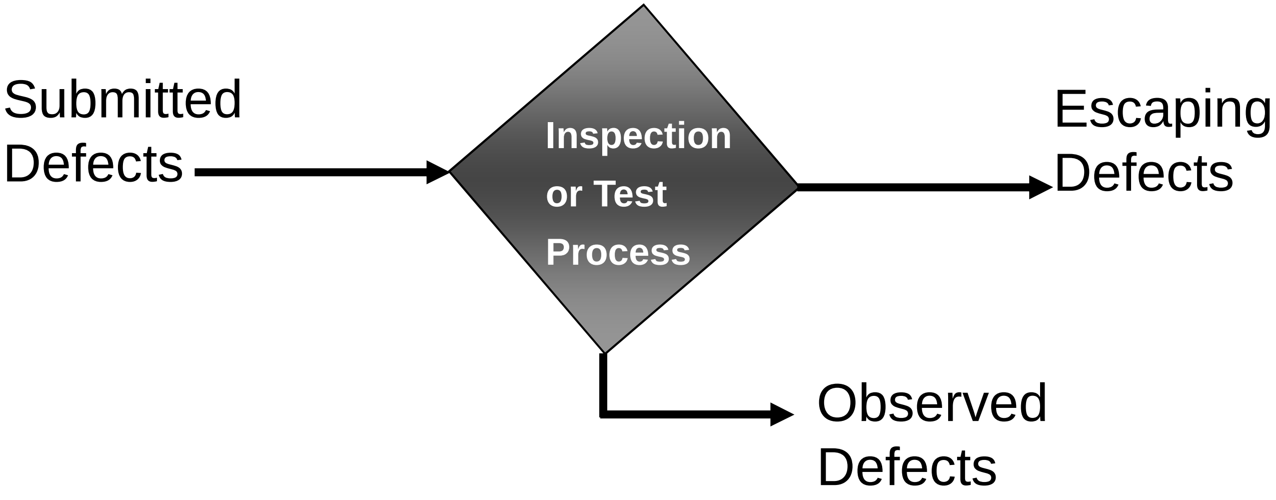
How can Defect Level Constraints be used in Process Design?

- Create a structured process flow diagram for the entire set of assembly operations for the product, identifying:
  - All inspection/test points.
  - Include the nonconforming product found at each inspection/test point.
- Establish maximum defect/unit level for the delivered product.
- Working from the start of the process to the end, estimate the defect/unit entering, escaping each process step using actual factory data and the effectiveness of the inspection or test process.

How can Defect Level Constraints be used in Process Design?

- If the estimated process delivery defect/unit is greater than the maximum allowed:
  - Revise the process flow where necessary by:
    - Redesigning the operations for increased process capability to produce fewer defects.
    - Implement Statistical Process Control and Design of Experiments (DOE) to reduce process variation.

Inspection or Test Process Effectiveness



Submitted Defects

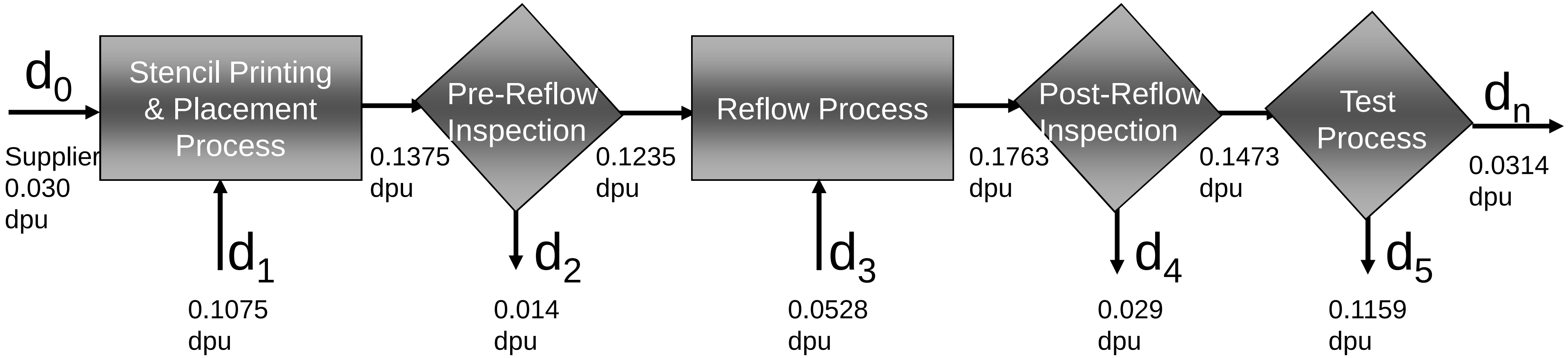
Inspection or Test Process

Escaping Defects

Observed Defects

	Submitted	Observed	Escapes
Defects	1,487	152	1,335
dpu	0.1375	0.014	0.1235
Effectiveness	10.22 % = (152/1,487) * 100		

Inspection & Test Planning



d_0

Supplier 0.030 dpu

Stencil Printing & Placement Process

d_1

0.1075 dpu

0.1375 dpu

Pre-Reflow Inspection

d_2

0.014 dpu

0.1235 dpu

Reflow Process

d_3

0.0528 dpu

0.1763 dpu

Post-Reflow Inspection

d_4

0.029 dpu

0.1473 dpu

Test Process

d_5

0.1159 dpu

d_n

0.0314 dpu

	Pre-IR Inspection		**Post-IR Inspection**		**Test Process**	
	Observed	**Escapes**	**Observed**	**Escapes**	**Observed**	**Escapes**
Defects	**152**	**1,335**	**317**	**1,588**	**1,251**	**340**
dpu	**0.014**	**0.1235**	**0.029**	**0.1473**	**0.1159**	**0.0314**
Effectiveness	**10.22 %**		**16.64 %**		**78.62 %**	

Inspection & Test Planning: Summary

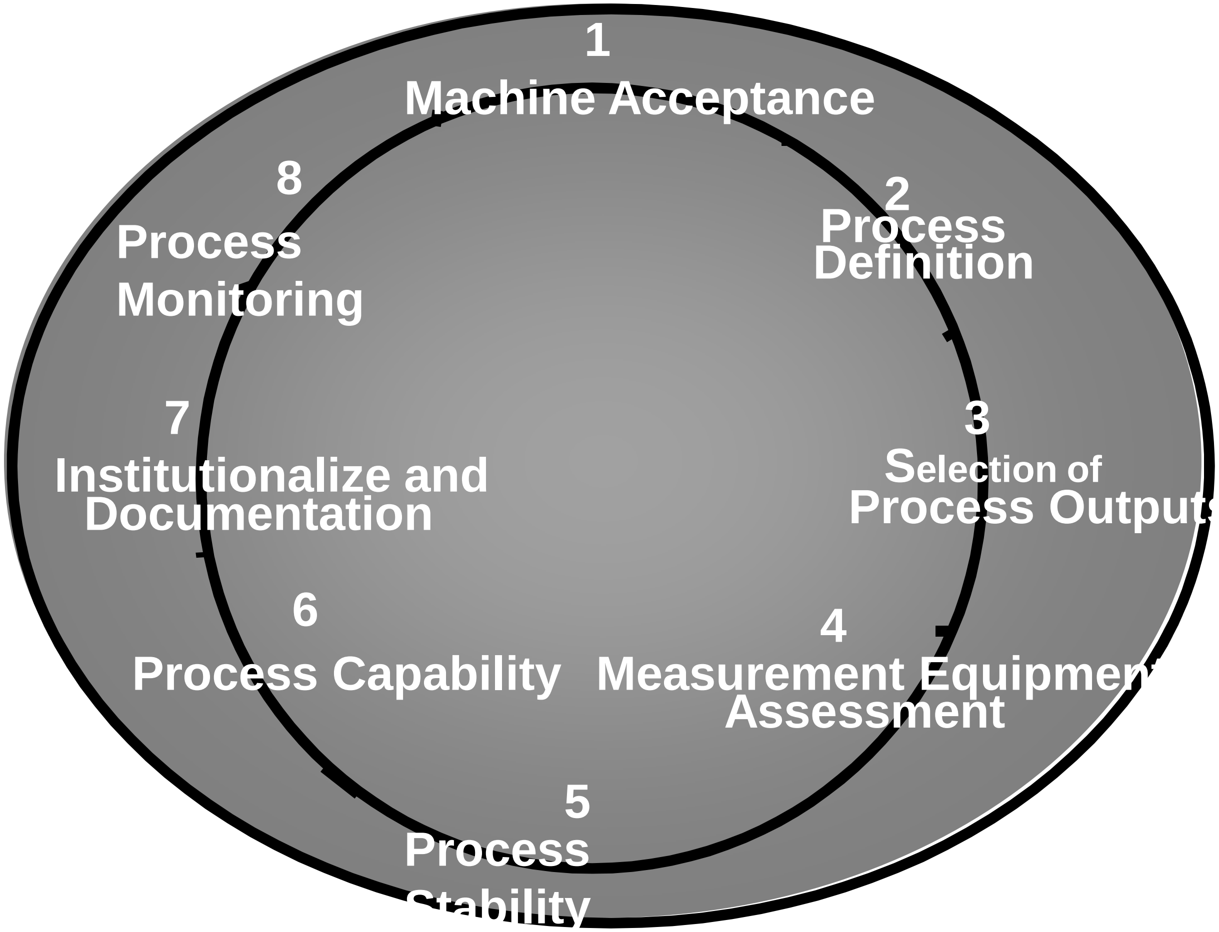
- Eliminating defects is the most important key to achieving a World - Class Manufacturing Operation.
- Defects per unit is the best measure of actual total product quality because it allows prediction, analysis, planning and benchmarking by product / process development teams

Process Characterization Concepts

Process Characterization

- Process Characterization is a technique to identify and minimize sources of variation in our processes and to obtain an understanding of the quantitative effects of the process inputs on the process outputs.
- Statistical methods are employed throughout the process characterization program to isolate sources of variation to meet stability and capability requirements.

Eight Steps to Process Characterization



1
Machine Acceptance

2
Process Definition

3
Selection of Process Outputs

4
Measurement Equipment Assessment

5
Process Stability

6
Process Capability

7
Institutionalize and Documentation

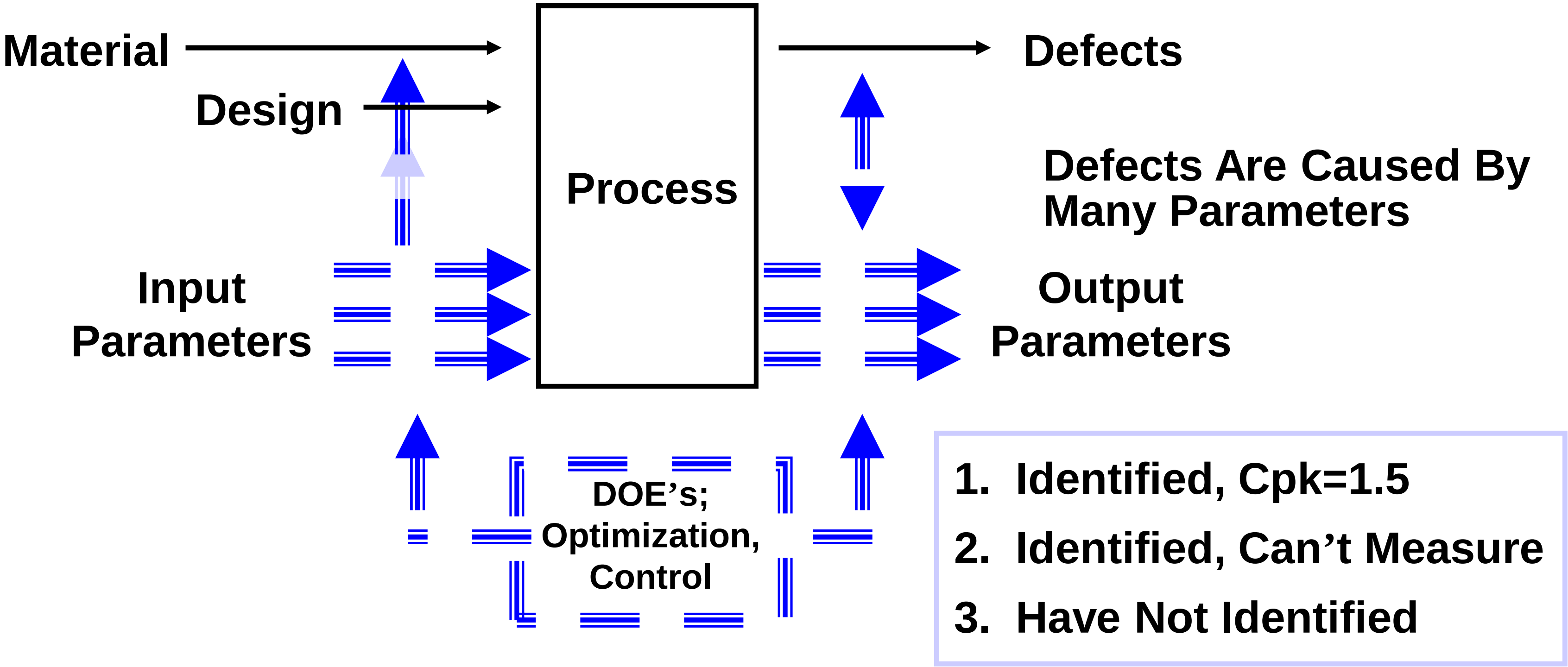
8
Process Monitoring

Machine Acceptance Studies

“Prevention” vs. “Reaction”

- Statistically confirms machine operation
- Reduces special cause variation due to machine operation
- Minimizes loss of production time
- Minimizes machine down time

Defect Reduction Methodology Process Characterization Approach



Material

Design

Process

Defects

Defects Are Caused By
Many Parameters

Input
Parameters

Output
Parameters

DOE’s;
Optimization,
Control

1. Identified, Cpk=1.5
2. Identified, Can’t Measure
3. Have Not Identified

Evidence of Process Characterization Methodology

- Process Focus
- Attribute and Variable Data
- Terminology of Cp/Cpk’s
- Identifying Process Parameter to Study
- Performing Capability Studies
- Optimizing the Process
- Implementing Process Controls
- Identifying Additional Critical Parameters
  - Reuse Of Other Facilities’ Findings
  - Use of DOE’s & Statistical Methods Apparent
- Correlating Parameters to Actual Process Improvement

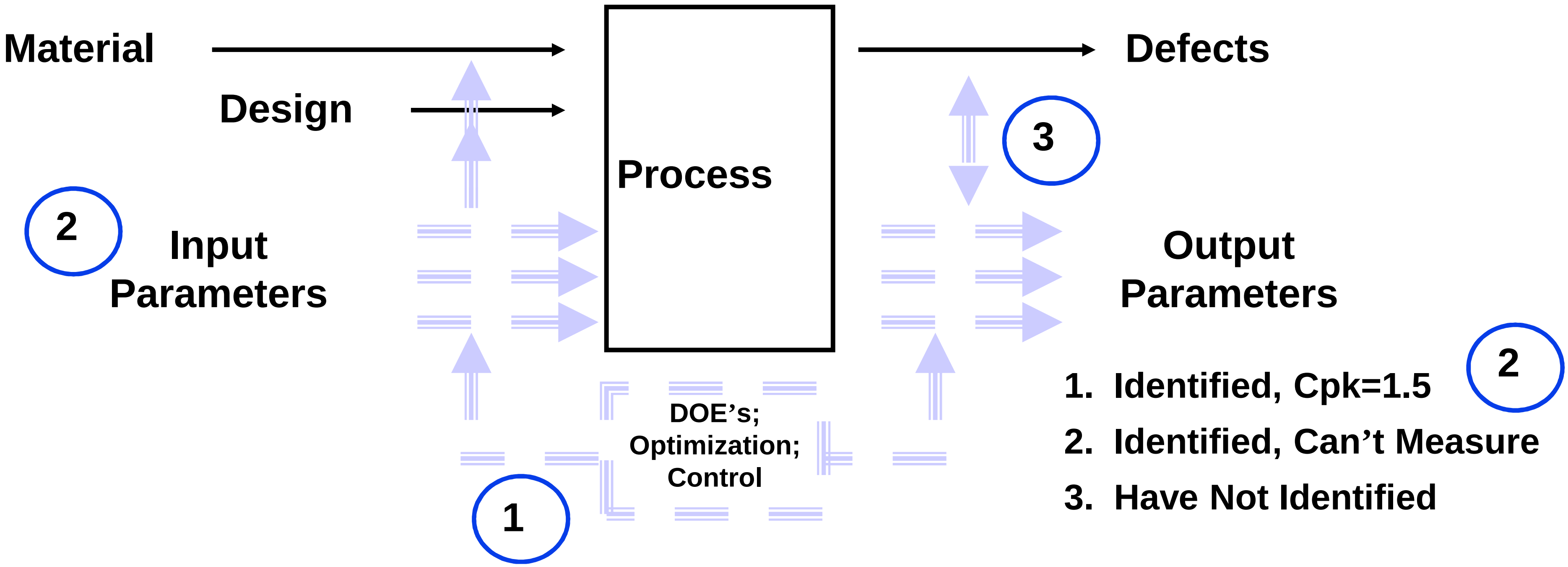
Process Characterization Methodology

- Is a way of understanding, controlling and coping with variability - that is managing variability.
    - Management Commitment to Statistical Data Analysis and Problem Solving
    - Implement Statistical Process Control (SPC) to monitor key process parameters
    - Daily Quality Meetings
    - Root Cause Corrective Actions
    - Measurement Systems Analysis
    - Design of Experiments
    - Continuous Process Improvements
    - SPC Audits

Process Characterization Methodology

- Results:
  - Reducing Defect Rate (dpu), Cycle Time, Repair costs, and increasing Productivity.
  - Increasing the time the process is in an ideal state.
  - Decreasing the process variability.
  - Increasing the time that the process characteristics mean remains at its target value or remains constant at acceptable level.
  - Reducing the number of out of control conditions on SPC .

Intent and Expectation
Quality Goals



1. Identified, Cpk=1.5
2. Identified, Can't Measure
3. Have Not Identified

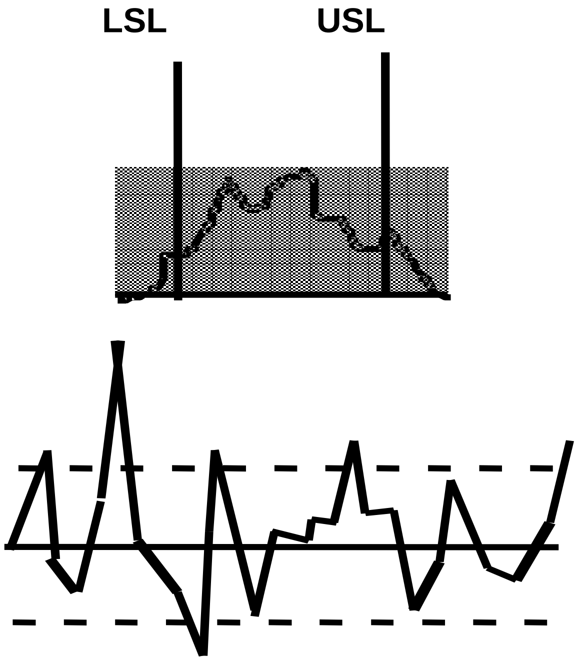
1. Institutionalize statistical methods based problem solving techniques

2. It is more important to identify (and control) additional parameters that have an impact on actual process performance than to pursue parameters that have a low impact on actual process performance .

3. Quality reviews should address the impact of process characterization efforts on reducing DPU. This is expected to be qualitative at first and should become quantitative as time progresses.

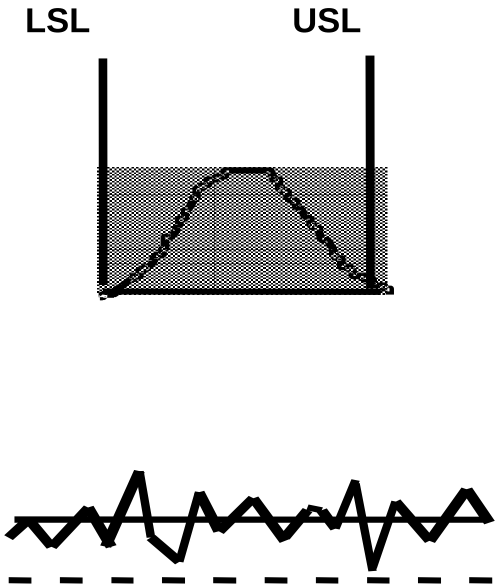
Evolution of Continuous Improvement in the Reduction of Variation

Before Using Statistical Methods



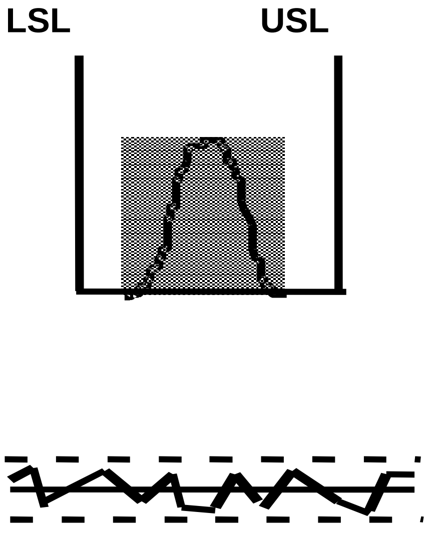
The Process is not in control, not predictable.

SPC Implementation



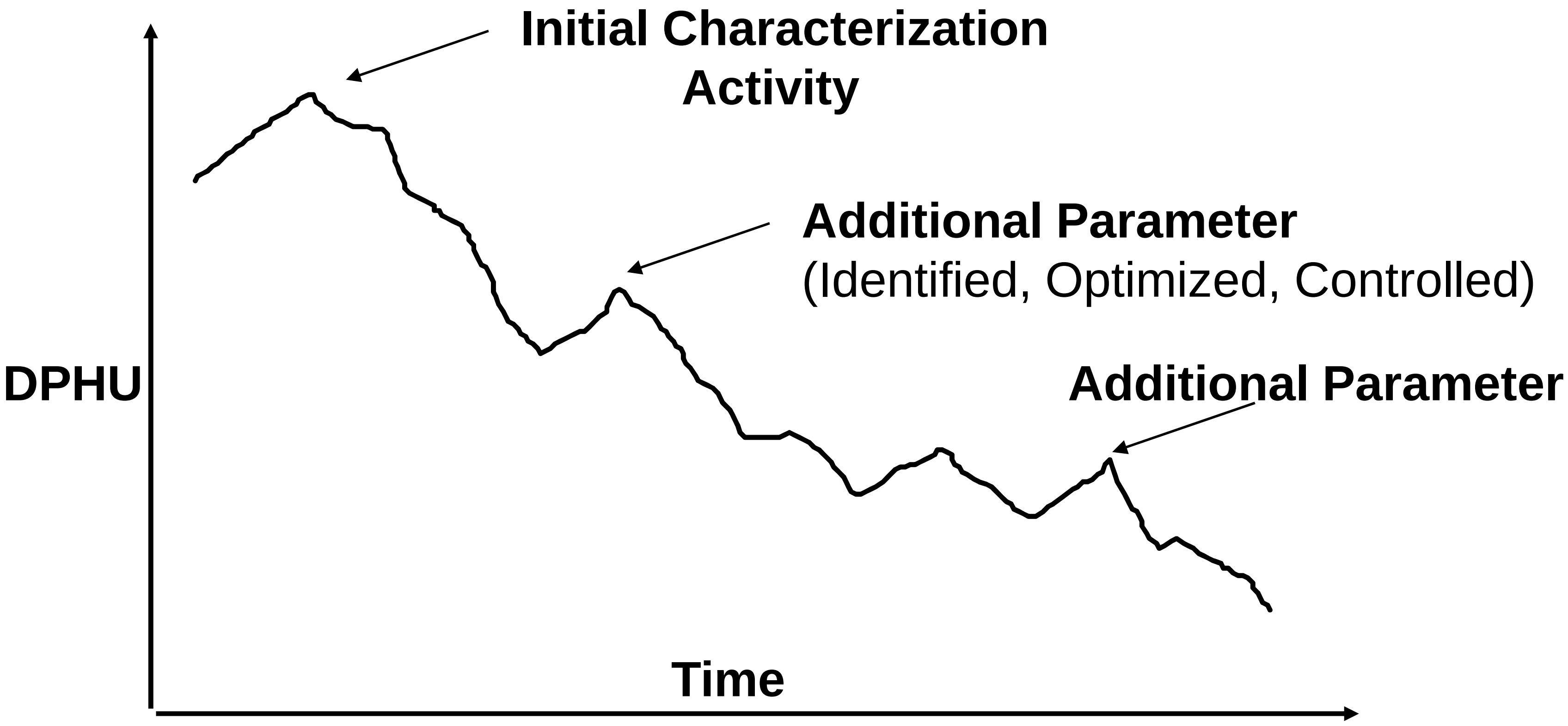
Using SPC, the process is in control, but its capability is poor.

Utilizing Design of Experiments



Using DOE & problem Solving techniques, the process capability has improved.

Link Process Characterization to DPHU Efforts



Initial Characterization Activity

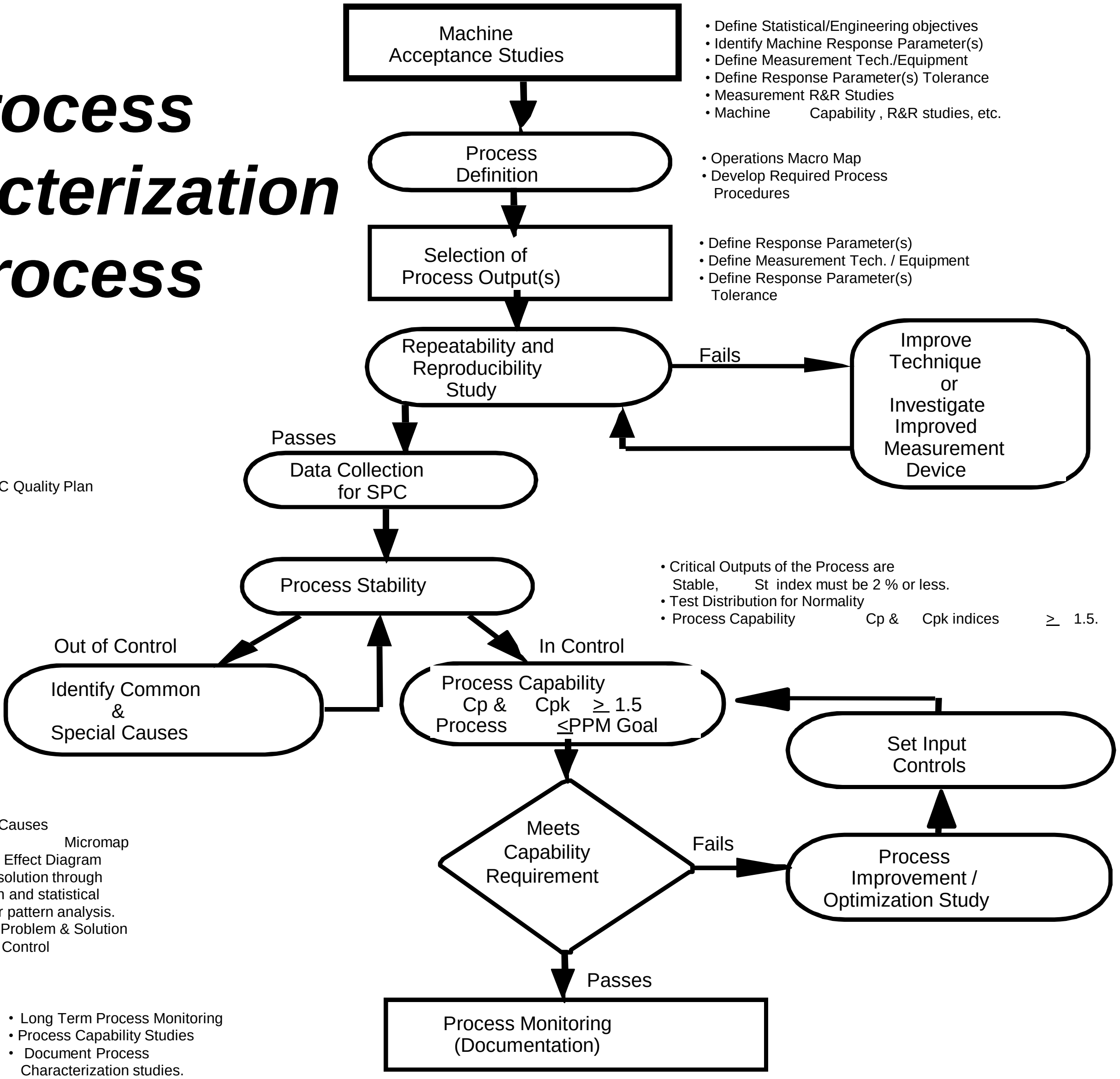
Additional Parameter
(Identified, Optimized, Controlled)

Additional Parameter

Continuous Improvement Activity in a Process Characterization Environment

- Involves:
  - Reducing the number of out of control conditions.
  - Increasing the time the process is in an ideal state.
  - Decreasing the process variability.
  - Increasing the time that the process characteristics mean remains at its target value or remains constant at some acceptable level.

Process Characterization Process



Machine Acceptance Studies:

- Define Statistical/Engineering objectives
- Identify Machine Response Parameter(s)
- Define Measurement Tech./Equipment
- Define Response Parameter(s) Tolerance
- Measurement R&R Studies
- Machine Capability , R&R studies, etc.

Process Definition:

- Operations Macro Map
- Develop Required Process Procedures

Selection of Process Output(s):

- Define Response Parameter(s)
- Define Measurement Tech. / Equipment
- Define Response Parameter(s) Tolerance

Data Collection for SPC:

- Develop SPC Quality Plan

Process Stability:

- Critical Outputs of the Process are Stable, St index must be 2 % or less.
- Test Distribution for Normality
- Process Capability Cp & Cpk indices ≥ 1.5.

Set Input Controls:

- Establish "Best" operating target and range for all critical input parameters.
- Implement Control Strategy for all Critical (input) Parameters and set to their optimal levels.

Process Improvement / Optimization Study:

- Achieve Quality Levels through Improvement / Optimization Studies.
- Define Critical Process (input) Parameter(s)

Identify Common & Special Causes:

- Identify Potential Causes
- Develop Process Micromap
- Develop Cause & Effect Diagram
- Test each cause/solution through experimentation and statistical data analysis or pattern analysis.
- Develop / Revise Problem & Solution matrix to Out of Control

Process Monitoring (Documentation):

- Long Term Process Monitoring
- Process Capability Studies
- Document Process Characterization studies.

Printing Positrol Diagram

To support the Process Characterization initiative, the following matrix of important characteristics should be available to process engineers for use in their respective processes as required to achieve defect reductions.

INPUT CHARACTERISTICS Supplier materials, methods, machine parameters and environment			
Important Characteristic	**Process Tolerance**	**Suggested Measurement Equipment**	**Suggested Process Control**
Solder Paste Viscosity	By paste type	Viscometer	X bar, R control charts
Stencil Aperture Width	Dependent upon Stencil Mfgr.	Micro view system	X bar, R control charts
Facility Temperature & Humidity	By paste type	Temp./Humidity gage	X bar, R control charts
Time solder paste sits on stencil	10 to 15 min.'s (Paste Dependent)	Equipment's paste knead or double print next board	Equipment's process software
Stencil Wash: IPA - % flux on Board	From supplier	Omega Meter	Process Log
Stencil Wash: Saponifier - Tritation	From supplier	Tritation kit from supplier	Process Log
Stencil Quality (Dents, cleanliness, wear & tear)	Not Applicable	Visual Inspection	Process Log & Audits
Support Tooling (Placement, Cleanliness, Wear & Tear)	Not Applicable	Visual Inspection	Process Log & Audits

Printing Positrol Diagram

OUTPUT CHARACTERISTICS
Produced by machine or operation

Important Characteristic	Process Tolerance	Suggested Measurement Equipment	Suggested Process Control
Solder Paste Height	8 mil +/- 2 mils	Cyber Sentry or SVS system	X bar, R control charts
	6 mil -1,+2 mils		
Solder Paste Coverage	+/- 10% Target	Equipment 2D system	Equipment's 2D error detection system
Process Defects & Errors	Not Applicable	Factory Reporting System, Trend Charts	U-Control chart by process, Pareto Charts,
Solder Paste Volume	+/- 30 % of Target	Cyber Sentry or SVS system	X bar, R control charts

OPERATOR DEPENDENT CHARACTERISTICS

Important Characteristic	Process Tolerance	Suggested Measurement Equipment	Suggested Process Control
Frequency of stencil wiping	Every 6 to 8 boards (Paste Dependent)	Not Applicable	Process audits or automatic wiping
Solder Paste Handling from refrigeration	Ambient for 24 hrs	Not Applicable	Process Log, date / time stamp paste container

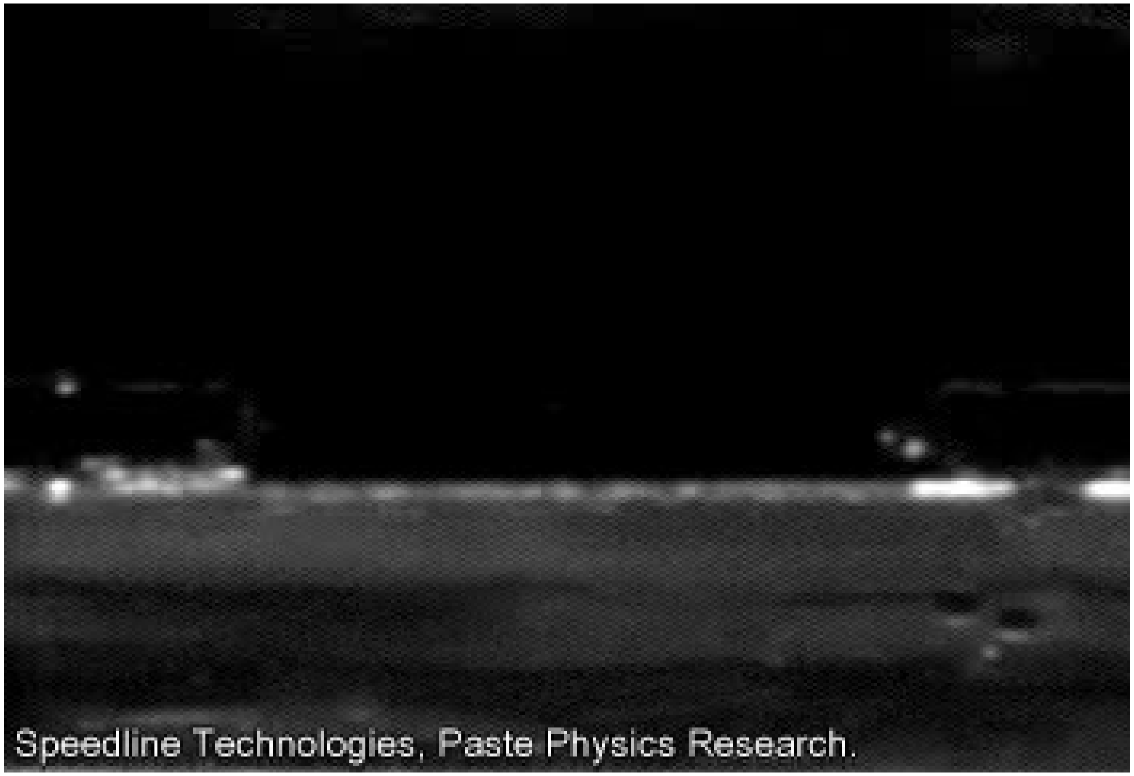
Printing Positrol Diagram

PREVENTATIVE MAINTENANCE CHARACTERISTICS			
Important Characteristic	**Process Tolerance**	**Suggested Measurement Equipment**	**Suggested Process Control**
Height of Support nest plate to base	Screen printer mfgr.	Height Gage	PM Logs & Audits
Stencil holder to base parallelism	Screen printer mfgr.	Height Gage	PM Logs & Audits
Blade Angle	Screen printer mfgr.	Calib. to 90 degrees	PM Logs & Audits
Force applied to right/left side of print head	Screen printer mfgr.	Calibration on control cards	PM Logs & Audits
Printer Cleanliness (Nest, Stencil, base, height sensor, etc.)	Not Applicable	Visual Inspection	PM Logs & Audits
Squeegee Blade (Dents and angle)	Not Applicable	Visual Inspection	Process Log & Audits

OTHER CHARACTERISTICS			
Important Characteristic	**Process Tolerance**	**Suggested Measurement Equipment**	**Suggested Process Control**
Operator Certification Program	Not Applicable	Not Applicable	Written and/or observation tests

Stencil Design

Paste Flow in Apertures

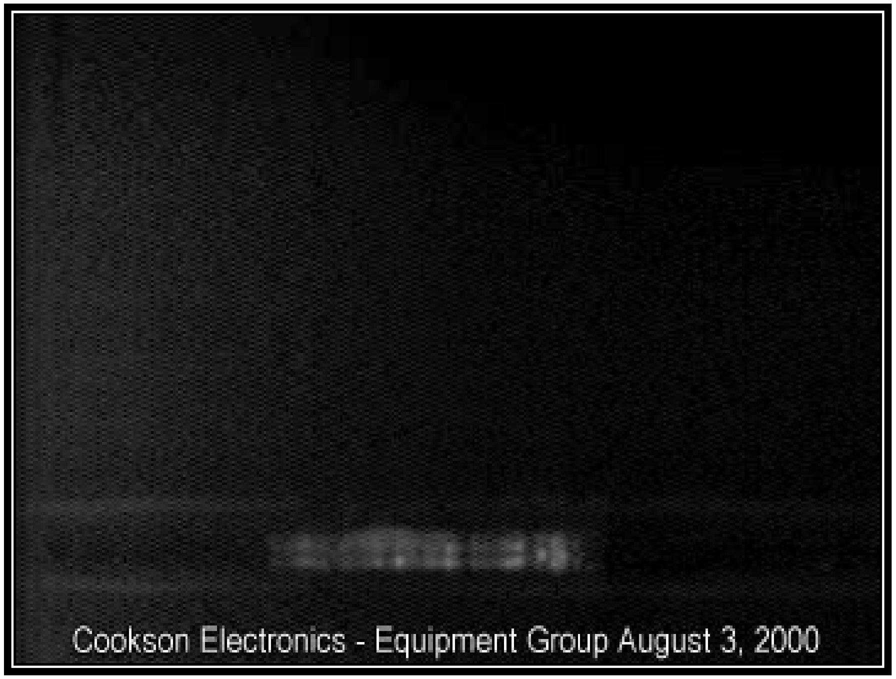

Speedline Technologies, Paste Physics Research.

- OMNIX 5000
- Poly Blade

- Type III Powder
- 25 mil Width

- 1.5 in/sec Print Speed
- 1.5 lb/in Squeegee Pressure

Solder Paste Release Performance



- 10 mil Diameter Aperture
- 0.1 in/sec Stencil Release Velocity

Design Rules For Stencils

There are two rules used in Stencil Design

- **Aspect Ratio Rule**
  - The aspect ratio rule has been used for a great deal of time in determining how well solder paste will transfer from the aperture to the surface of the printed circuit board

- **Area Ratio Rule**
  - As smaller components have been used in electronics products requiring smaller stencil apertures the area of the opening of the aperture and the area of the walls of the aperture have become closer requiring the use of the area ratio rule in stencil design

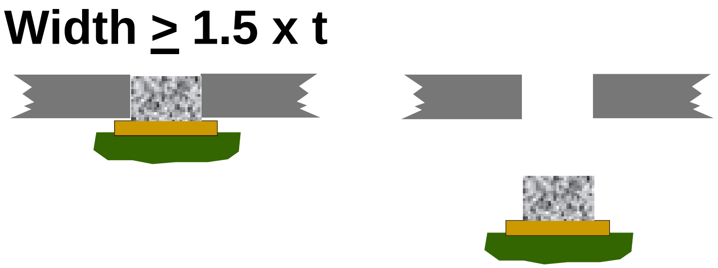
Aspect Ratio Rule

For Optimal Transfer Efficiency

Aspect Ratio

  - Ensures that the aperture will allow the printed material to release onto the substrate.
  - Aspect Ratio - W / t > 1.5 (chem-etch)
- For Example: 9 mil. aperture min. use 6 mil foil.

Violation of Aspect Ratio



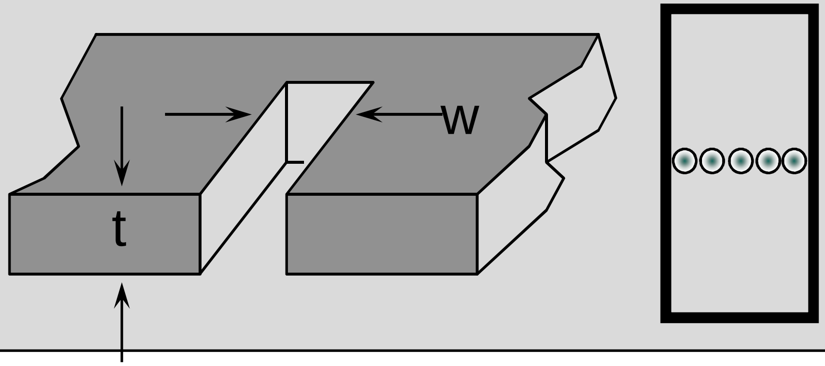
Correct Aspect Ratio

Stencils - Aperture Design

Typical Fine Pitch Apertures

Reduce aperture size by 20% to your pad size, maintain a minimum of 1.5 aspect ratio of aperture width to stencil thickness. (25mil pitch and Below).

Minimum Aperture Design Guidelines:



Aspect Ratio = W / t >1.5

Width >= 4-5 Particle Diameters

Design Rules For Stencils Aspect Ratio

For Fine Pitch QFP’s, Aspect Ratio Was The Limiting Factor for Printing:

Aspect Ratio is .. $\dfrac{\text{Aperture width} \quad (W_A)}{\text{Stencil Thickness } (T_S)}$

A Typical 0.4mm (16mils) Pitch QFP Aspect Ratio is … $\dfrac{9}{5} = 1.8$

However as the apertures have become smaller, the area of the opening of the aperture and the area of the aperture walls have become very much the same. Aspect Ratio alone is not the only stencil design calculation that must be used to insure an optimum stencil design. The Area Ratio must also be used.

Design Rules For Stencils Area Ratio

Area Ratio

$$\frac{\textbf{Area of the opening}}{\textbf{Area of the aperture walls}}$$

The holding force of the solder paste to the printed circuit board pad must be greater than the holding force of the solder paste to the stencil aperture for the solder paste to release from the aperture and attach to the printed circuit board pad

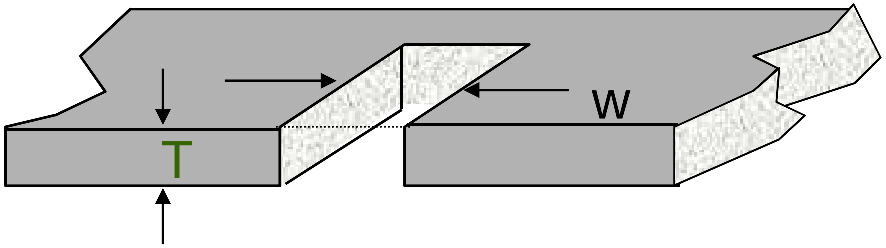
Area Ratio Rule

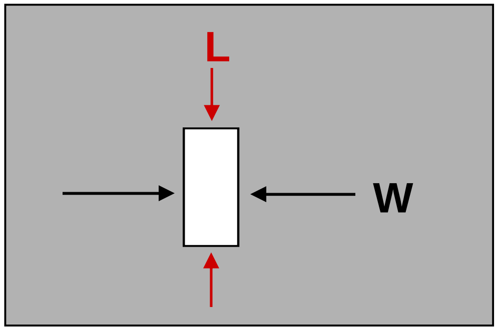
For Optimal Transfer Efficiency

Area Ratio

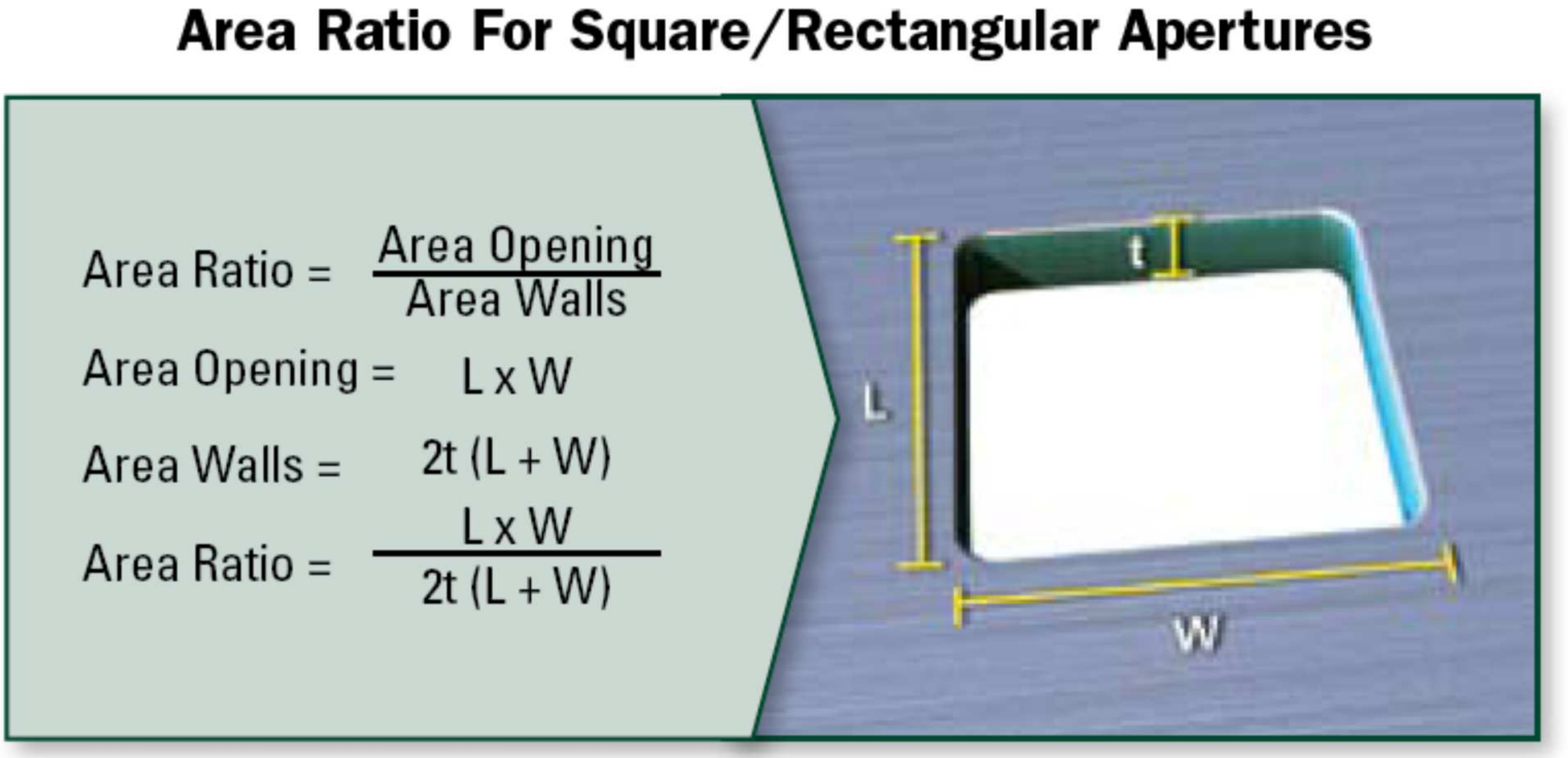
- Ensures that the forces pulling a material onto the pad are greater than the forces holding it in the aperture.

$$\frac{\text{Pad Pulling Tension (P)}}{\text{Retaining Wall Tension (R)}} = \frac{\text{Aperture (Length (L)} \times \text{Width (W))}}{\text{Stencil Thickness (T)} \times \text{Aperture Perimeter (2} \times \text{(L+ W))}} \geq 0.6$$





Area Ratio for Square and Rectangular Apertures



Area Ratio For Square/Rectangular Apertures

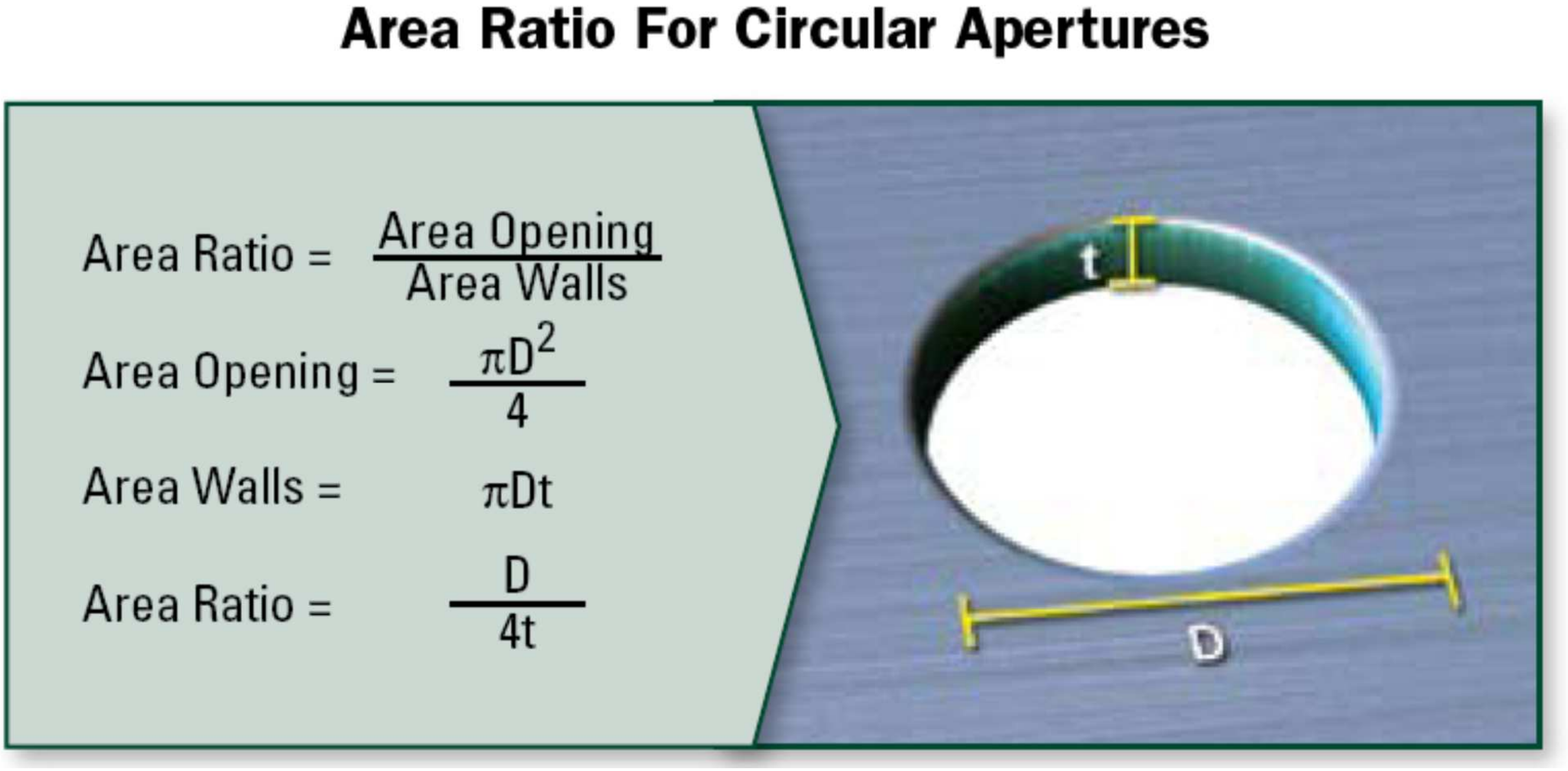
$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$

$$\text{Area Opening} = L \times W$$

$$\text{Area Walls} = 2t\,(L + W)$$

$$\text{Area Ratio} = \frac{L \times W}{2t\,(L + W)}$$

Area Ratio for Circular Apertures



Area Ratio For Circular Apertures

$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$

$$\text{Area Opening} = \frac{\pi D^2}{4}$$

$$\text{Area Walls} = \pi D t$$

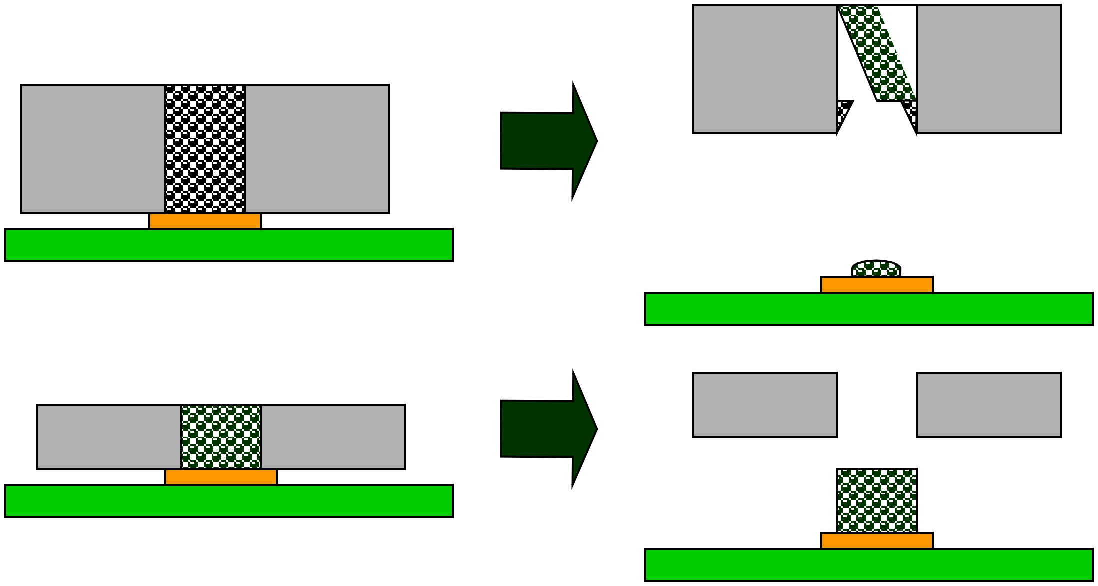
$$\text{Area Ratio} = \frac{D}{4t}$$

Why is Wall/Pad Ratio Important?

Area Ratio

- Key process feature for successful fine pitch printing is paste release from stencil….

1

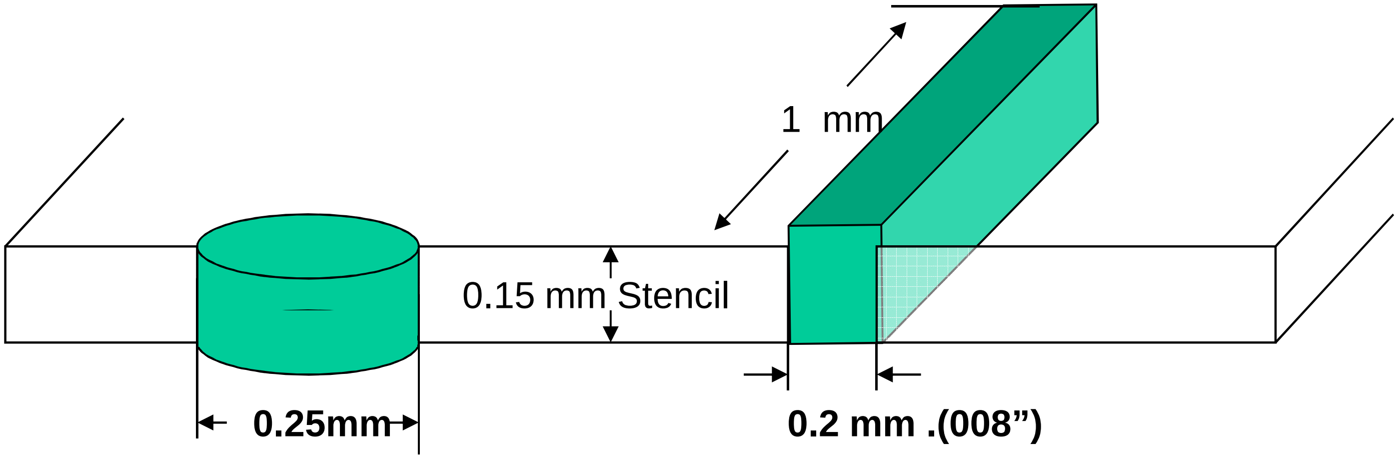


Violation of Area Ratio Rule

2

Correct Area Ratio

Comparing Aspect Ratio and Area Ratio



Circle

Aperture Wall Area = 0.118 mm^2
Pad Surface Area = 0.049 mm^2
Aspect Ratio = **1.67**
Surface Area Ratio = **0.42**

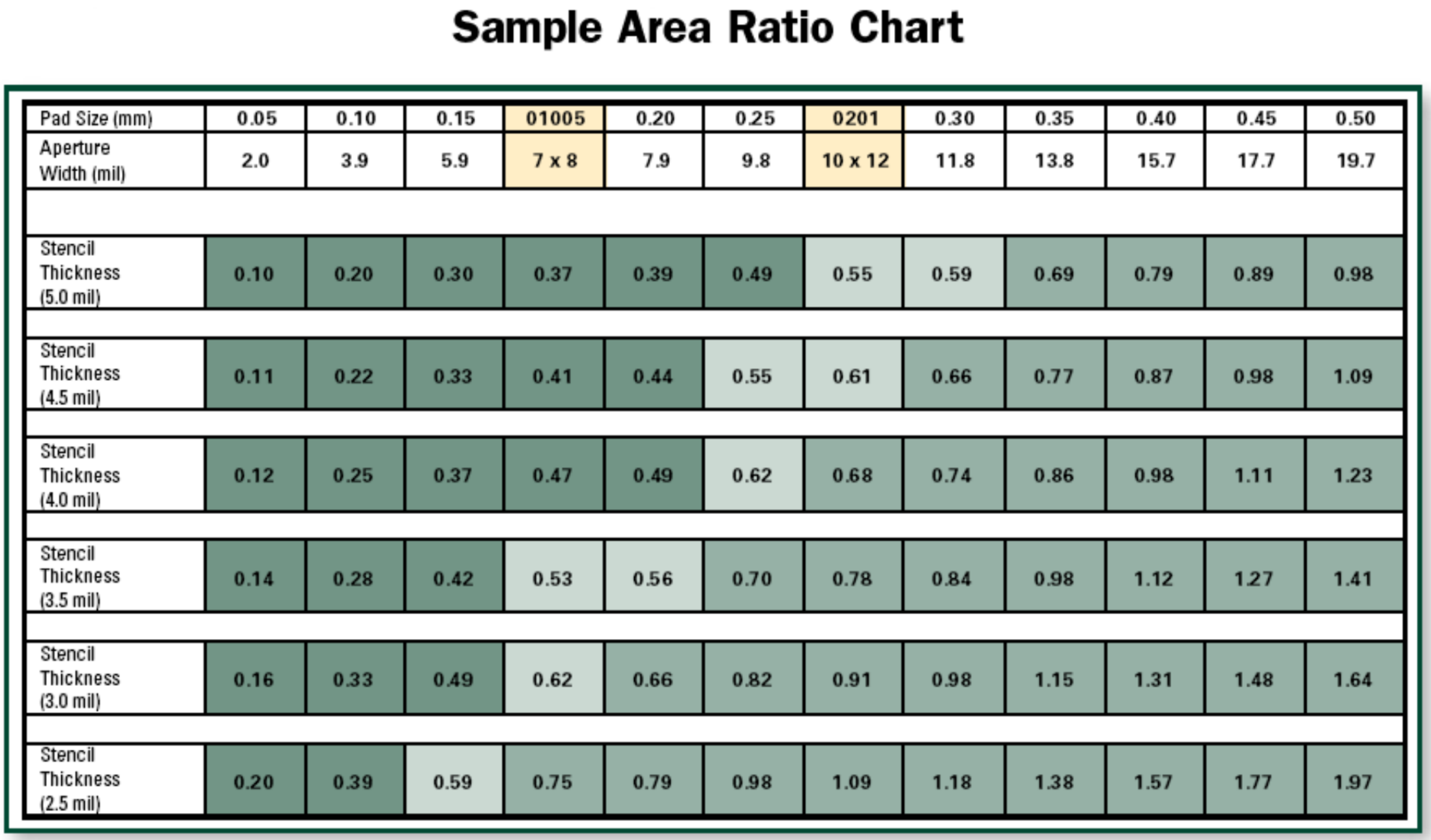
Rectangle

Aperture Wall Area = 0.36 mm^2
Pad Surface Area = 0.2 mm^2
Aspect Ratio = **1.34**
Surface Area Ratio = **0.56**

The circle is more difficult to print because of the lower Surface Area Ratio.

The aspect ratio is no longer a good indicator as here it suggests that the circle would be easier to print - it isn't

Sample Area Ratio Chart

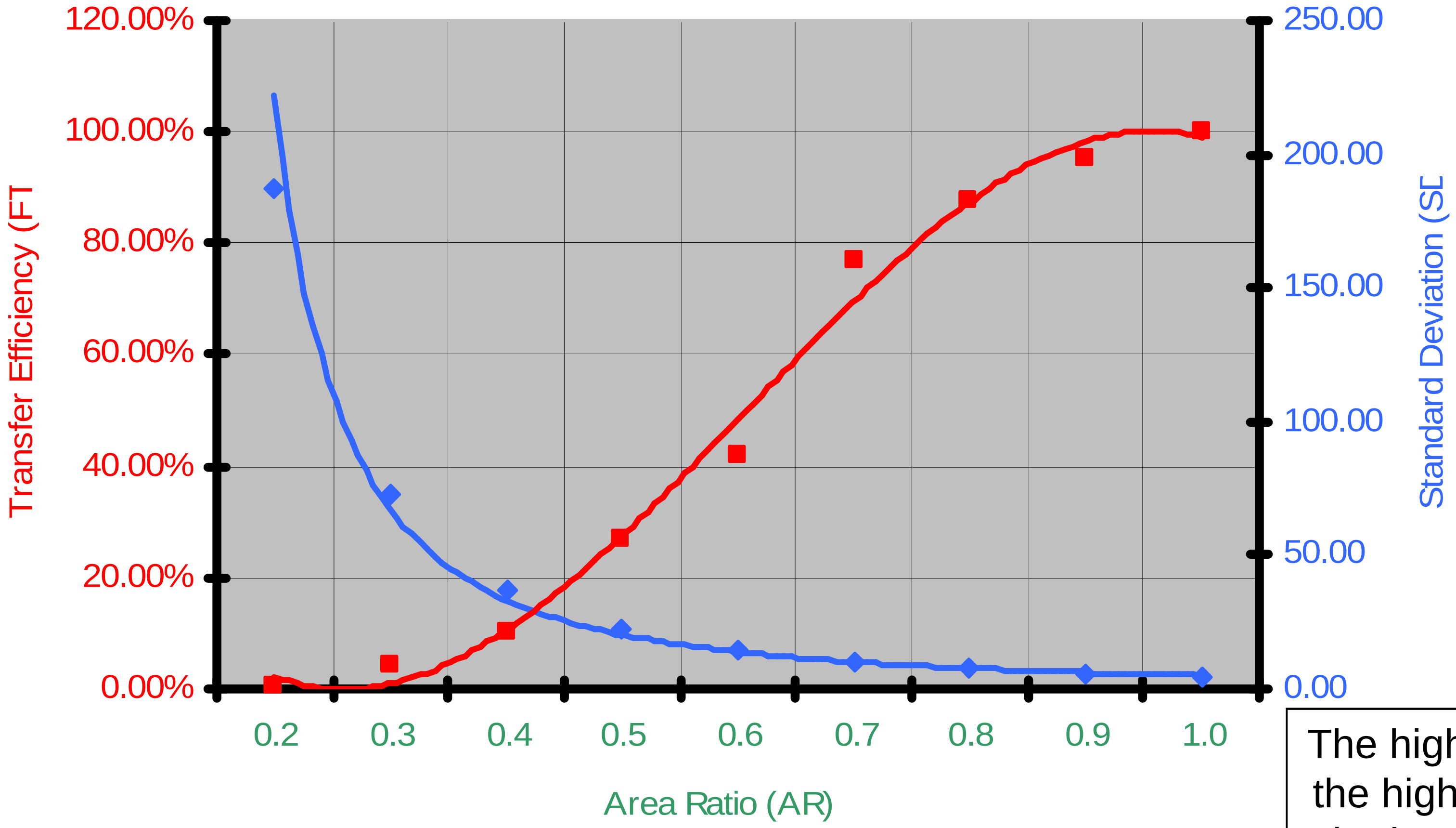


Sample Area Ratio Chart

Pad Size (mm)	0.05	0.10	0.15	01005	0.20	0.25	0201	0.30	0.35	0.40	0.45	0.50
Aperture Width (mil)	2.0	3.9	5.9	7 x 8	7.9	9.8	10 x 12	11.8	13.8	15.7	17.7	19.7
Stencil Thickness (5.0 mil)	0.10	0.20	0.30	0.37	0.39	0.49	0.55	0.59	0.69	0.79	0.89	0.98
Stencil Thickness (4.5 mil)	0.11	0.22	0.33	0.41	0.44	0.55	0.61	0.66	0.77	0.87	0.98	1.09
Stencil Thickness (4.0 mil)	0.12	0.25	0.37	0.47	0.49	0.62	0.68	0.74	0.86	0.98	1.11	1.23
Stencil Thickness (3.5 mil)	0.14	0.28	0.42	0.53	0.56	0.70	0.78	0.84	0.98	1.12	1.27	1.41
Stencil Thickness (3.0 mil)	0.16	0.33	0.49	0.62	0.66	0.82	0.91	0.98	1.15	1.31	1.48	1.64
Stencil Thickness (2.5 mil)	0.20	0.39	0.59	0.75	0.79	0.98	1.09	1.18	1.38	1.57	1.77	1.97

Relationship:

Transfer Efficiency
Area Ratio
Standard Deviation



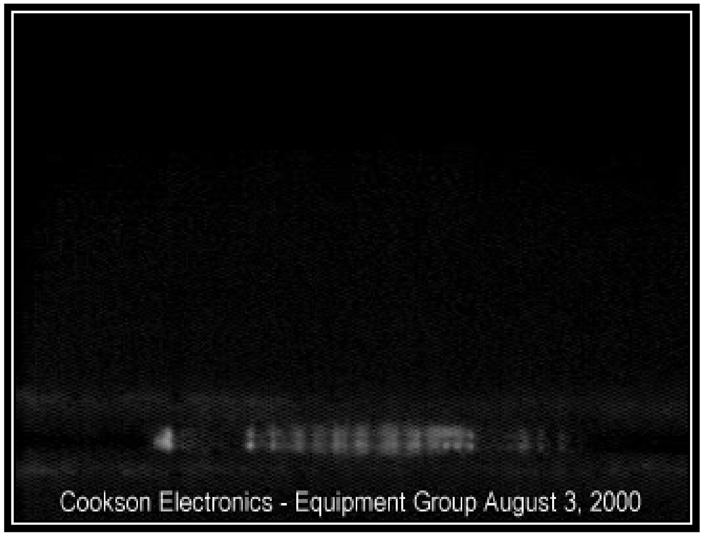
The higher the relative AR,
the higher the relative FT,
the lower the absolute SD

Reduction of Aperture Size

25 mil

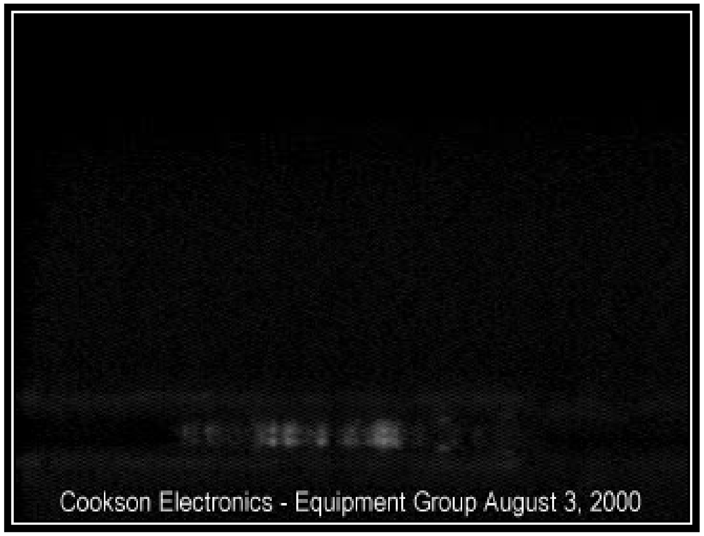
Cookson Electronics - Equipment Group August 3, 2000

20 mil



Cookson Electronics - Equipment Group August 3, 2000

15 mil



Cookson Electronics - Equipment Group August 3, 2000

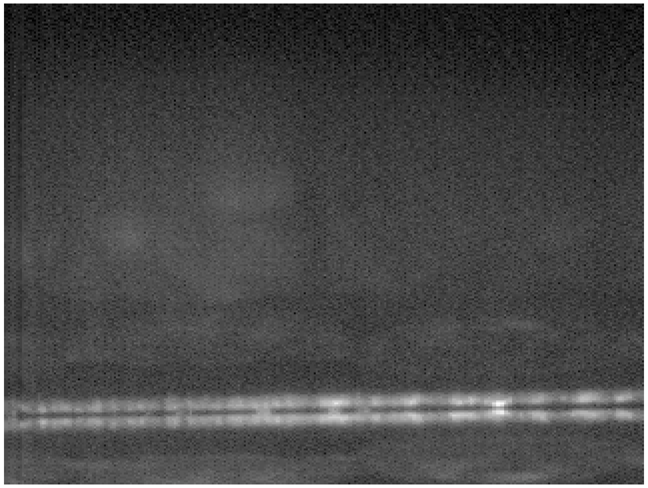
10 mil

Cookson Electronics - Equipment Group August 3, 2000

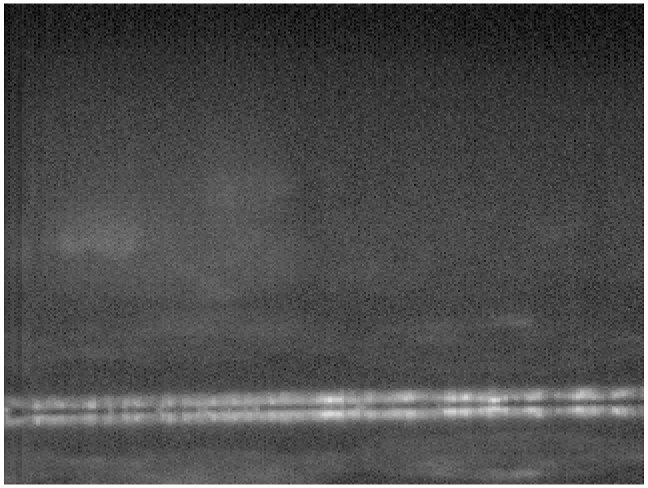
Paste Release for a 15 mil (.015") Circle

15 mil (.38 mm) Dia. Circle (Area Ratio = 0.96)

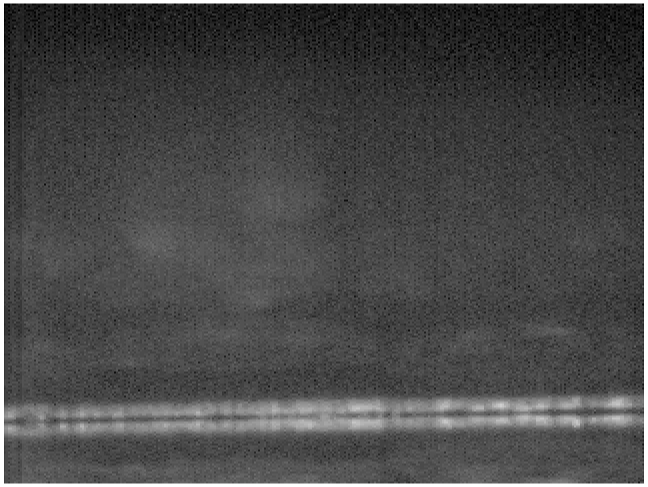
Paste 'A' SnPb



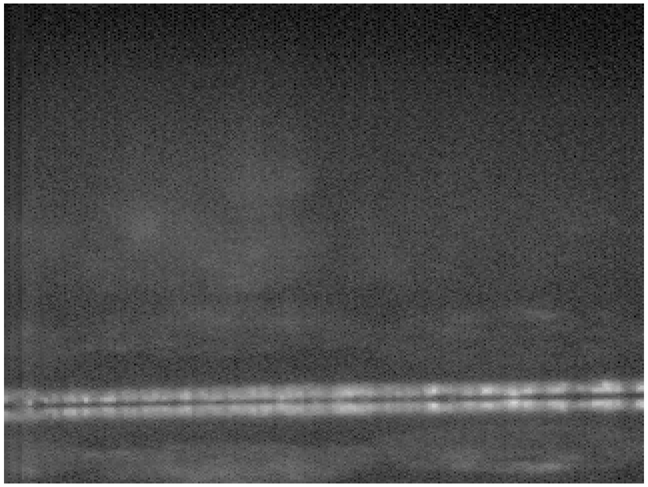
Paste 'A' Lead Free



Paste 'B' SnPb



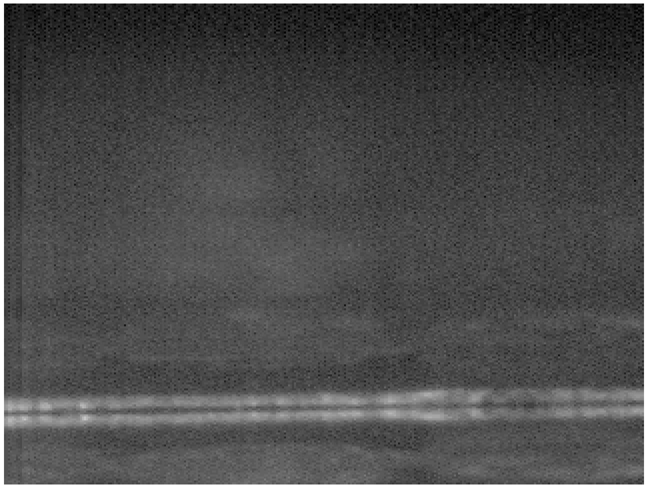
Paste 'B' Lead Free



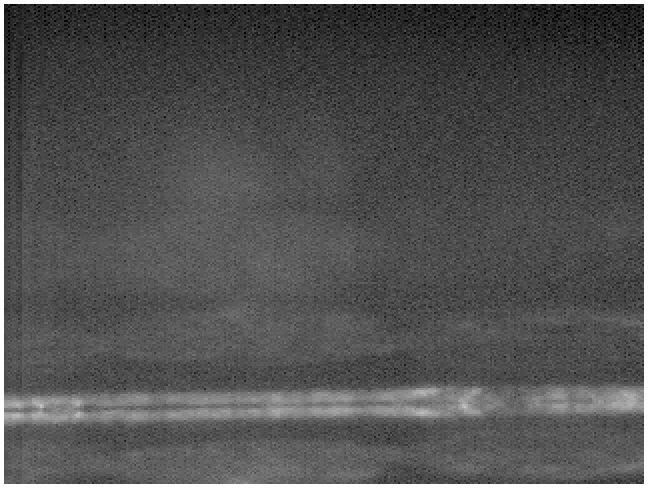
Paste Release for a 10 mil (.010") Circle

10 mil (.25 mm) Dia. Circle (Area Ratio = 0.64)

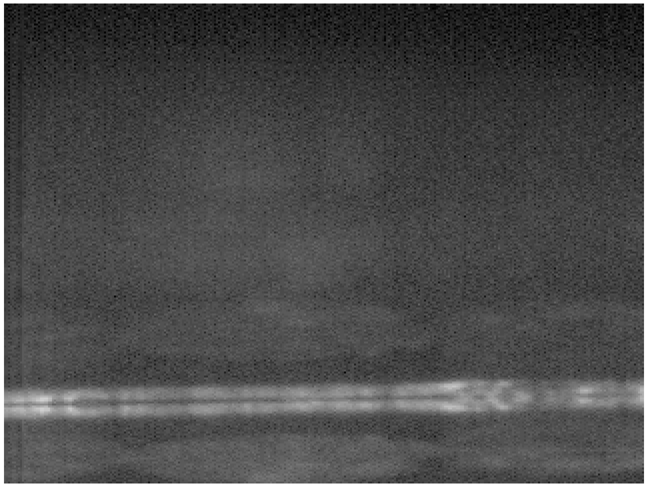
Paste 'A' SnPb



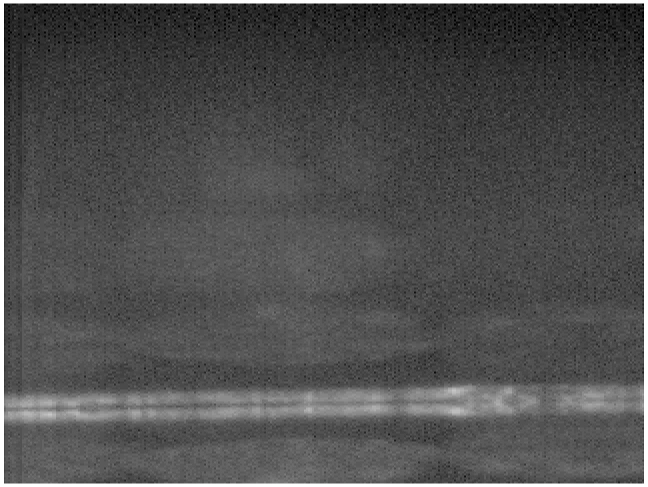
Paste 'A' Lead Free



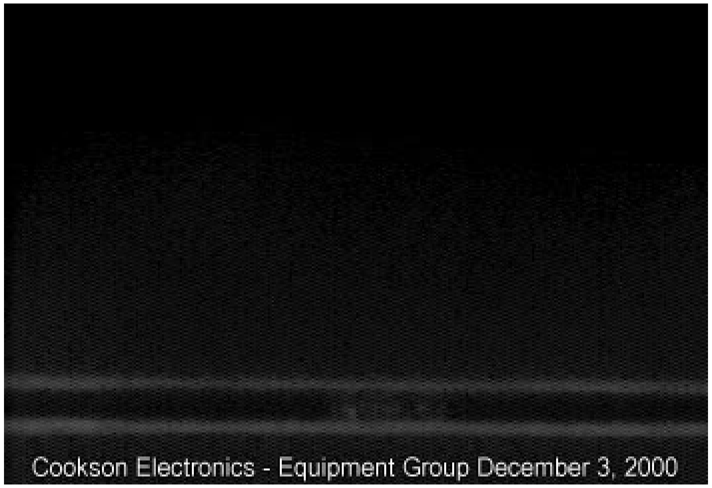
Paste 'B' SnPb



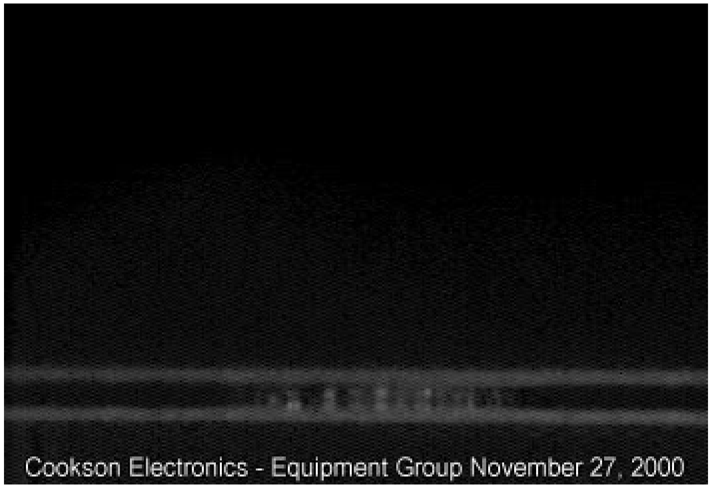
Paste 'B' Lead Free



Low Area Ratio Solder Paste Release

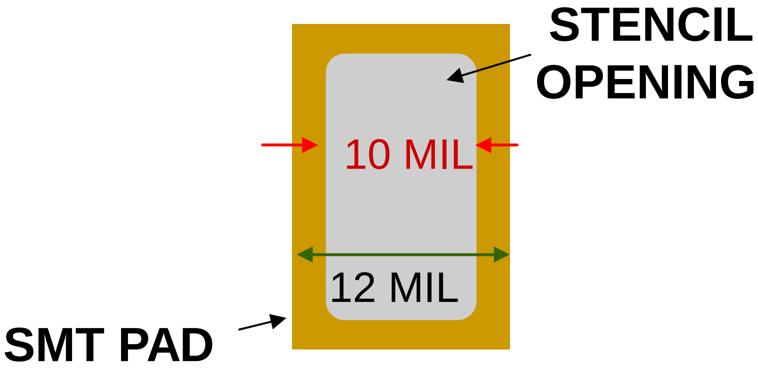


High Area Ratio Solder Paste Release



Print to Pad Ratio “Gasketing”

- **The ratio between the aperture width and pad should be at least 1:1.2**
  - Often called ‘Aperture Reduction’
  - EXAMPLE: 20 MIL (.5mm) Pitch Component



12 x 0.80 = 10 mil aperture

Aperture to Pad Alignment

- PCB Pads Over-etched
  - Making them smaller than the size in the Gerber data.
    - For boards that are over-etched, Good gasketing is ensured by reducing the size of the aperture to the pad

- Printed Circuit Board Tolerance

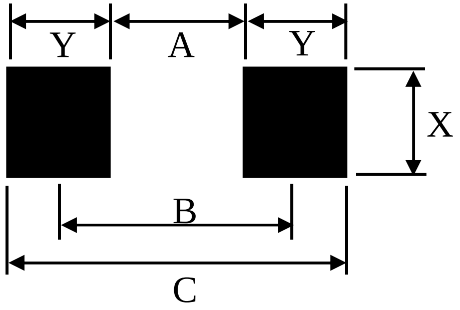
- Machine Alignment Tolerance
  - Stencil to PCB
  - Even the most accurate printing equipment has an alignment tolerance

- Stencil Tolerance

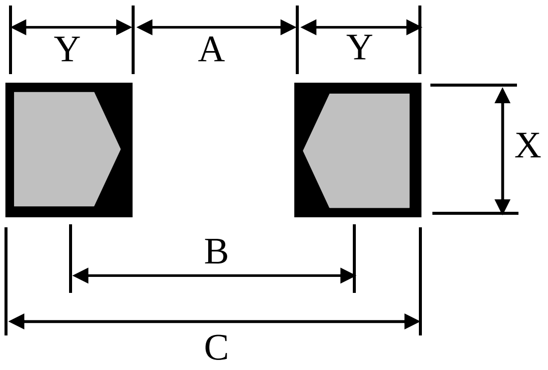
Stencil Design

Land Pattern & Aperture Design for 2-sided components

Land Pattern



Aperture Design



C = L(max) + 0.030”

A = L(min) - 2 x T(max)

X = W(max) + 0.010”

Y = (C-A) / 2

D = 0.75 * Y

F = X - 0.002”

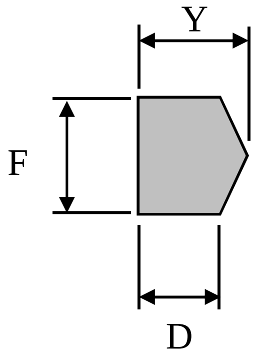
B = pad pitch

L(max) and (min) are the part length tolerances

W(max) is the part width tolerance

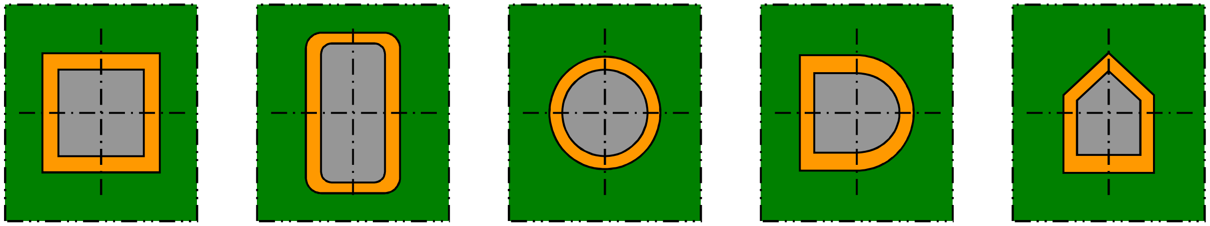
T(max) is the part thickness tolerance

The “Home Plate” design for chips was created to assist in reducing the effect of Solderballing when using No-Clean solder pastes, when too much paste is applied and too much solder is trapped beneath the part.

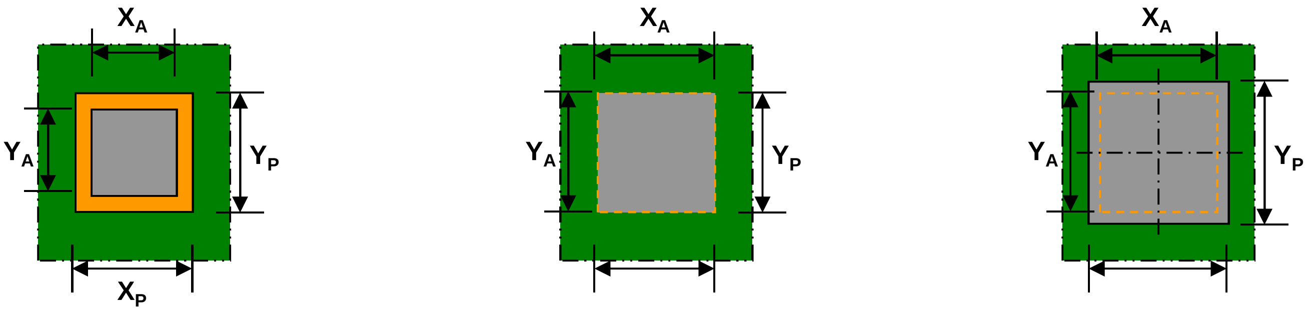


Aperture Modifications (examples)

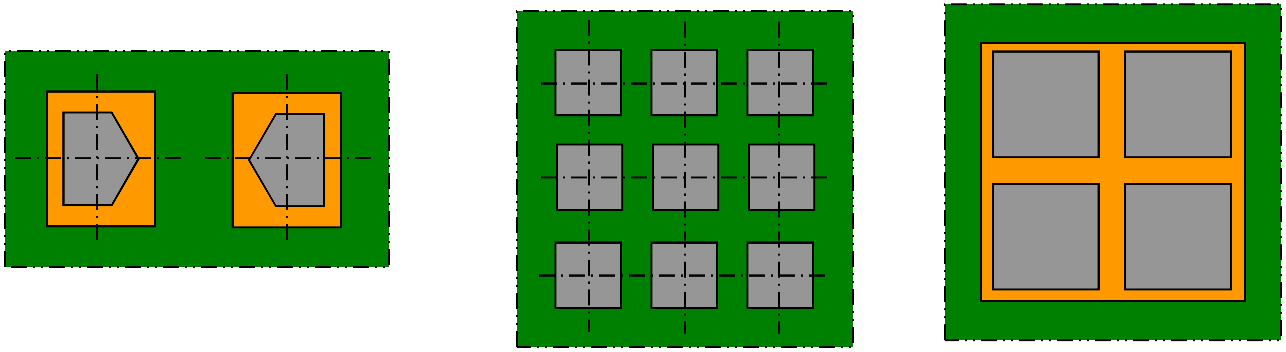
Shapes



Size



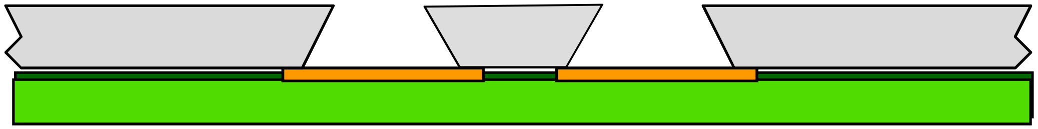
Exceptions



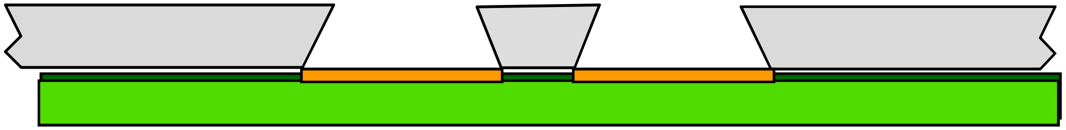
Poor Gasketing: Stencil Design

- **The speed at which squeeze out accumulates is dependent on the width of aperture relative to the pad**
  - Apertures reduced relative to the pad width will minimize squeeze out and prevent bridging.

Reduced

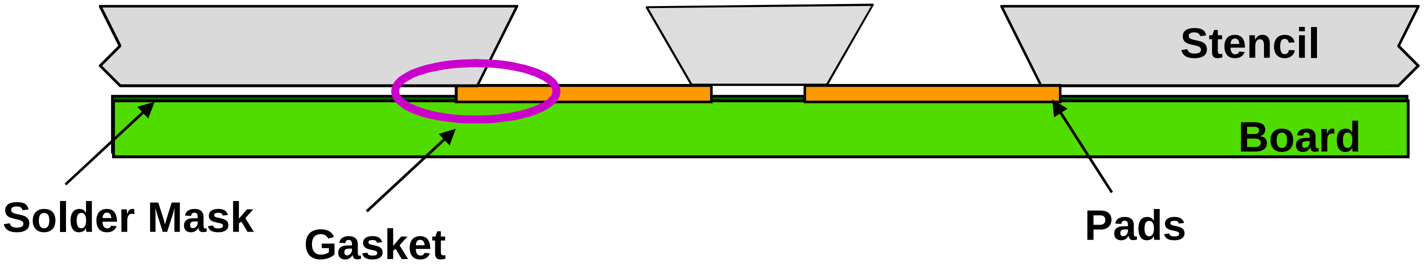


Not Reduced



Gasketing (Sealing)

- The contact of the PWB and stencil form a ‘gasket’ or seal between the stencil aperture and the printed circuit board component pad.
  - If the gasket is broken, solder shorts will occur.



Pad & Aperture Size Recommendations

English Units

Pitch	Pad Width	Aperture	Stencil thick	A.R.
.025”	.015”	.012”	.006”	2.0
.020”	.012”	.009-.010”	.005-.006”	1.7
.016”	.010”	.007-.008”	.005”	1.4
.012”	.008”	.005-.006”	.004-.005”	1.2

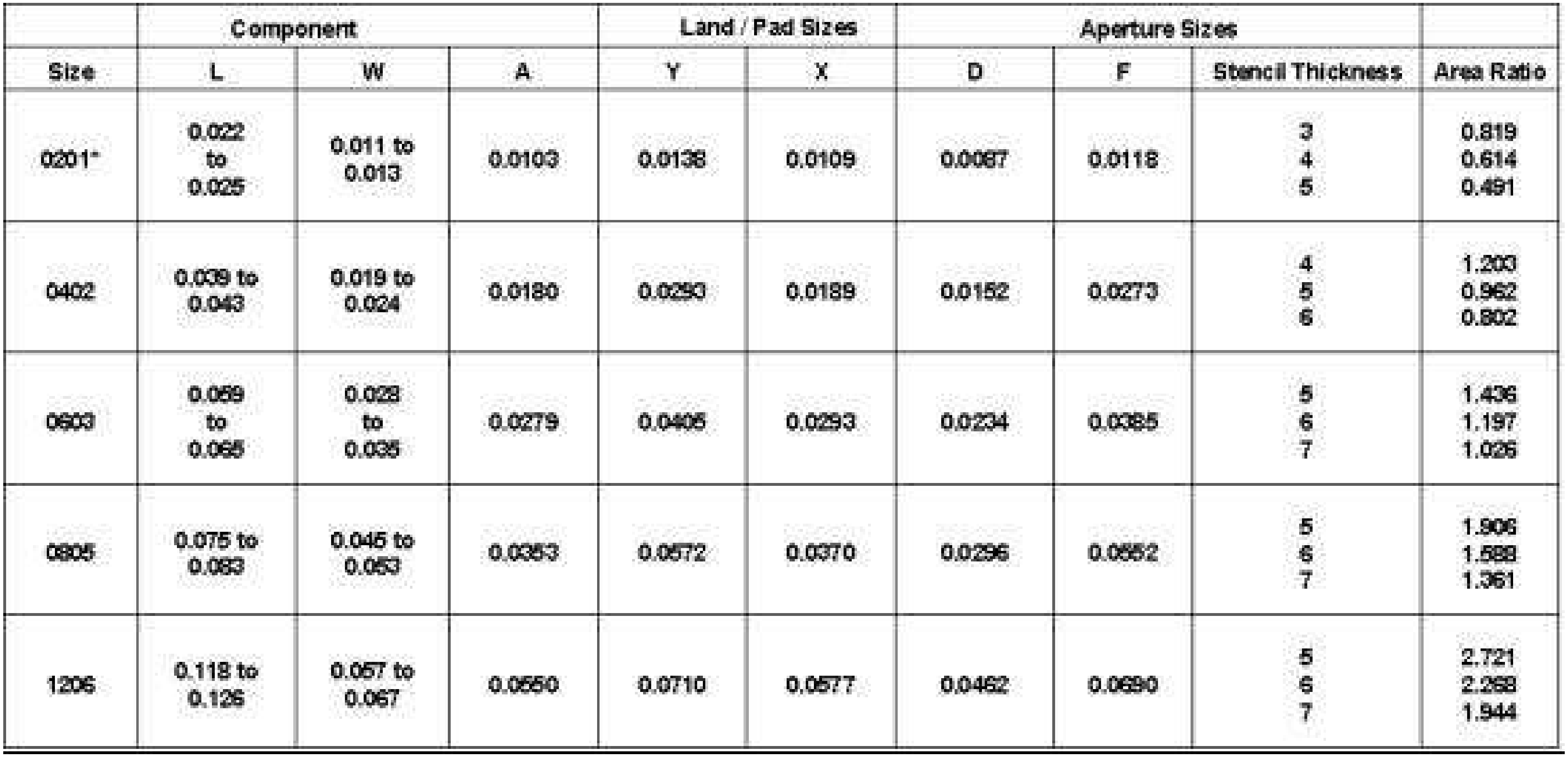
Pad & Aperture Size Recommendations

Metric Units

Pitch	Pad Width	Aperture	Stencil thick	A.R.
.64 mm	.38 mm	.30 mm	.15 mm	2.0
.51 mm	.30 mm	.23-.25 mm	.127-.15 mm	1.7
.41 mm	.25 mm	.18-.20 mm	.127 mm	1.4
.30 mm	.20 mm	.127-.15 mm	.1-.127 mm	1.2

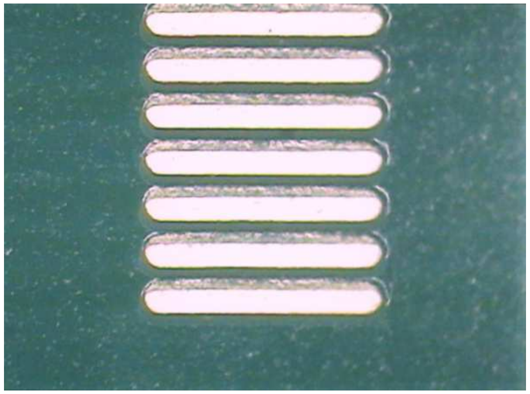
Stencils – Passive Devices

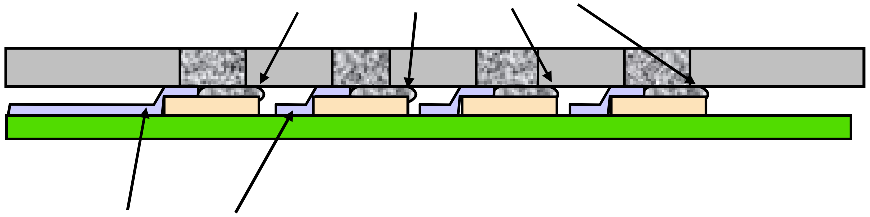
Common Resistor Sizes, Land Patterns, and Stencil Openings (from IPC-SM-782) specifications)



	Component			Land / Pad Sizes		Aperture Sizes			
Size	L	W	A	Y	X	D	F	Stencil Thickness	Area Ratio
0201*	0.022 to 0.025	0.011 to 0.013	0.0103	0.0138	0.0109	0.0087	0.0118	3 4 5	0.819 0.614 0.491
0402	0.039 to 0.043	0.019 to 0.024	0.0180	0.0290	0.0189	0.0152	0.0273	4 5 6	1.203 0.962 0.802
0603	0.059 to 0.065	0.028 to 0.035	0.0279	0.0406	0.0293	0.0234	0.0385	5 6 7	1.436 1.197 1.026
0805	0.075 to 0.083	0.045 to 0.053	0.0353	0.0572	0.0370	0.0296	0.0552	5 6 7	1.906 1.588 1.361
1206	0.118 to 0.126	0.057 to 0.067	0.0550	0.0710	0.0577	0.0462	0.0690	5 6 7	2.721 2.268 1.944

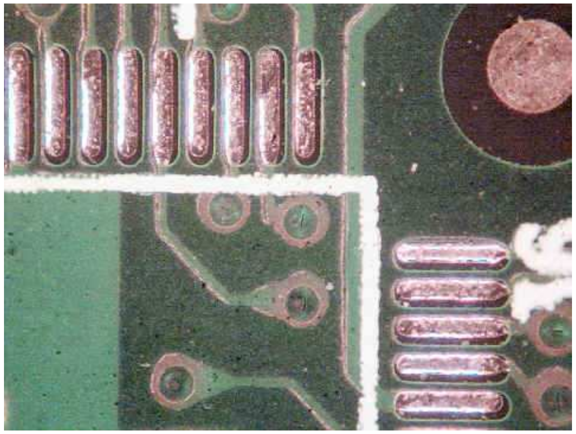
Board / Mask Problems

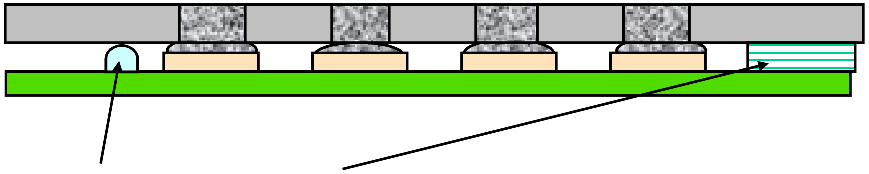




Paste Bleed out

Solder Mask over Pads

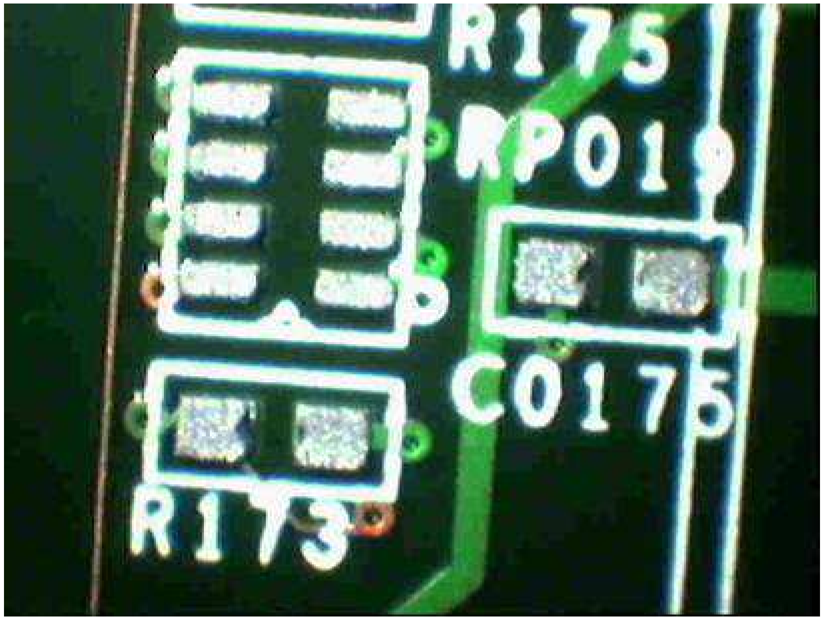




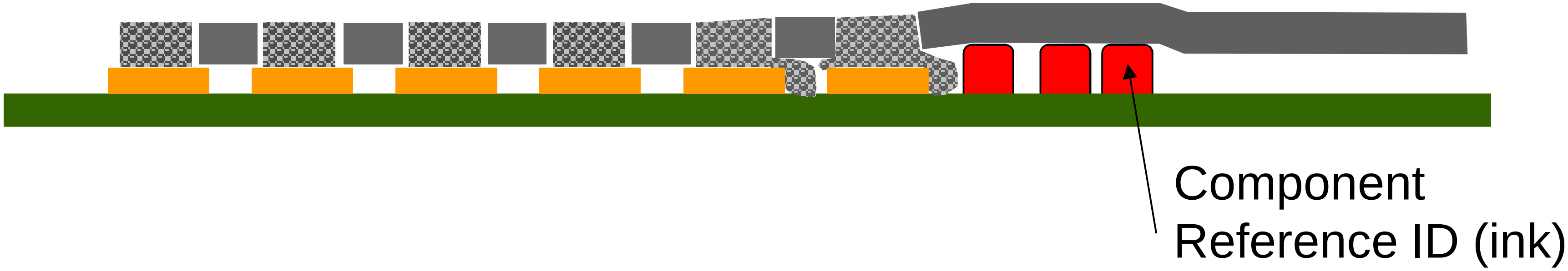
Silkscreen, and labels can prop up the stencil and prevents good gasketing which causes bleed out.

Board Legends

- **Labels or legends can also cause gasket problems**



Legend, Trace and Silkscreen is too high



Cookson Stencil Design Principles

1. Keep aperture shape the same as pad shape, unless otherwise required (by volume or process requirements)
   - Maximized board to stencil alignment repeatability
2. Apply absolute aperture reduction relative to pad
   - Maximized board to stencil alignment repeatability (2x -1 mil around)
3. Center aperture on pad
   - Maximized board to stencil alignment repeatability
4. When maximizing volume, use squares over circles
   - Maximizes volume (4/π greater volume then circles) while minimizing pitch issues
5. Area Ratio is main factor for paste release (see FIG 1)
   - Highest Area Ratio’s (≥ 0.66) provide Lowest Standard Deviation on Transfer Efficiency

Cookson Stencil Design Principles

6. Medium taper gives best transfer efficiency (smallest standard deviation)
    - Taper of 0.8 ± 0.2 mil provide Highest Transfer Efficiency with the Lowest Standard Deviation.
7. Aperture Design Modifications are independent from stencil manufacturing technique
    - Recommend thinner foil thickness (-5%) for ALPHA FORM stencils due to increased Transfer Efficiencies.
8. Component Technology ≤ 20 mil pitch and or Stencil Thickness ≤ 4 mil use ALPHA FORM Electroforming Technology
    - Highest volume deposits with lowest standard deviations measured under these circumstances with POS
9. Use Custom Shapes for discrete components
    - A 66% home plate design to increase process window by improving component alignment & outgassing, reduce squeeze balls & tombstoning effects.

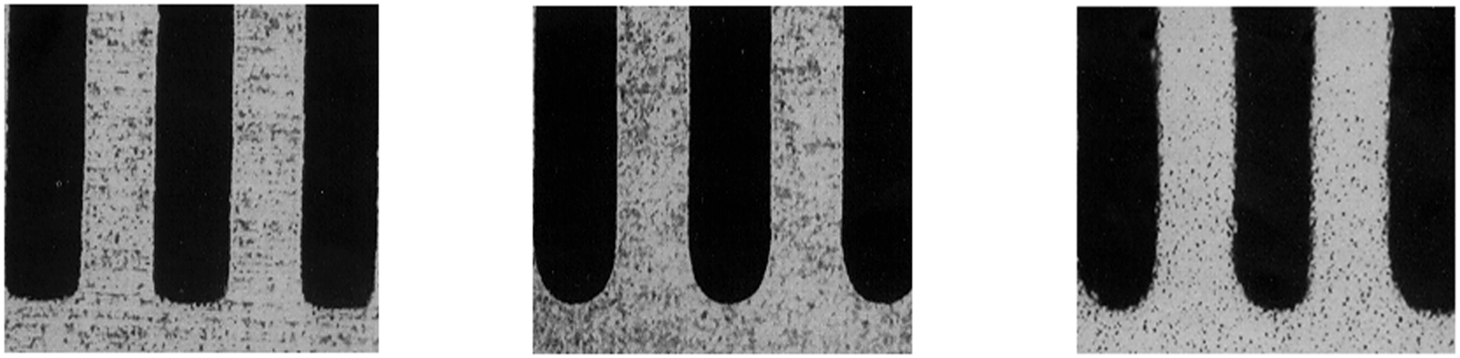
Cookson Stencil Design Principles

10. Area Array type of packages require Square Apertures
    - Maximizes volume (4/π greater volume then circles) while minimizing pitch issues
    - Different rules apply for fine feature BGA's
11. Solder Spreading Characteristics require different aperture design modifications
    - No aperture reductions for Lead Free Alloys and Water Soluble Pastes: they don't spread to the edges of the pads and will leave exposed pad finish
12. Stencil Thickness & Use of Steps will be determined by the smallest aperture and the largest aperture
    - Using the stencil thickness look-up tables based on pad sizes and Aspect Ratio (1:1.5)
13. Large apertures require support bars to prevent scooping, squeegee damage and voids.
    - Apertures ≥ 150 mil in X and/or Y require support bar 20 mil in X and/or Y.

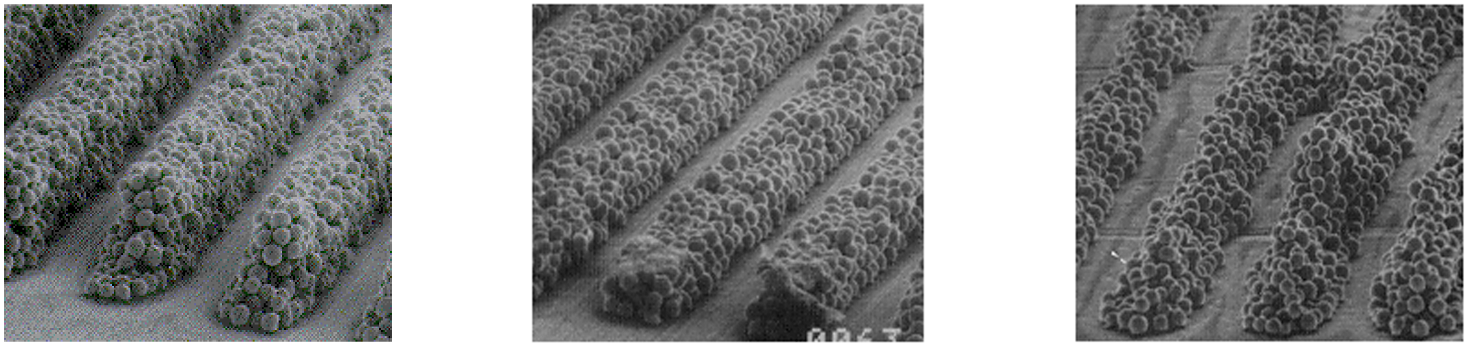
Cookson Stencil Design Principles

14. Stepped area's required offset angle to prevent squeegee damage
    - Steps should be rotated using a -5° angle
15. Frame less stencils should be considered
    - Consistent tension provides improved positional accuracy and reduced variation
    - Stencil storage space reduction
16. Aperture Orientation is a factor in stencil design
    - 45° Is neutral, however, altering 0° or 90° apertures would be below manufacturing tolerances and is therefore not significant
17. Squeegees and enclosed print heads is not a factor in stencil design
    - No data (yet) to design specific design rules
18. Reversed Taper only for experimental use
    - No data (yet) to design specific design rules

Common Stencil Types



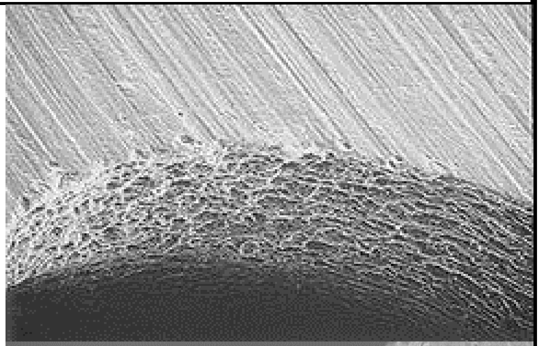
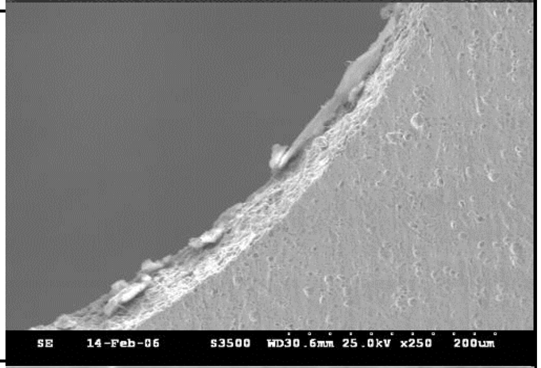
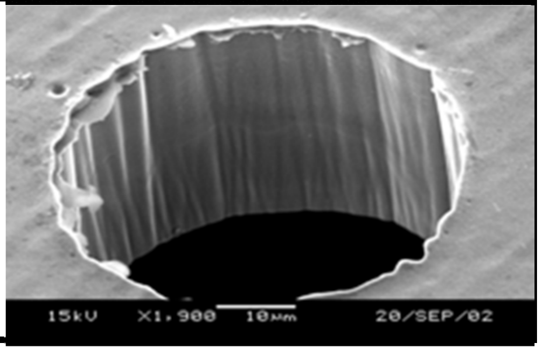
Stencil aperture (0.007” X 0.0875”) at 10X



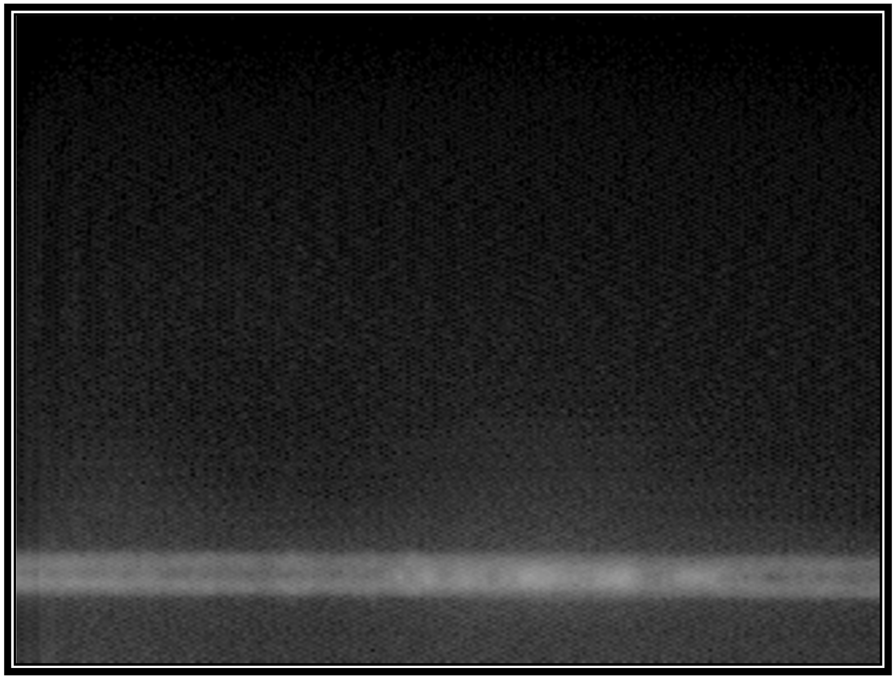
Electroplated **Laser cut** **Chemical etched**

Stencil aperture definition will impact paste deposition volume and defect rate

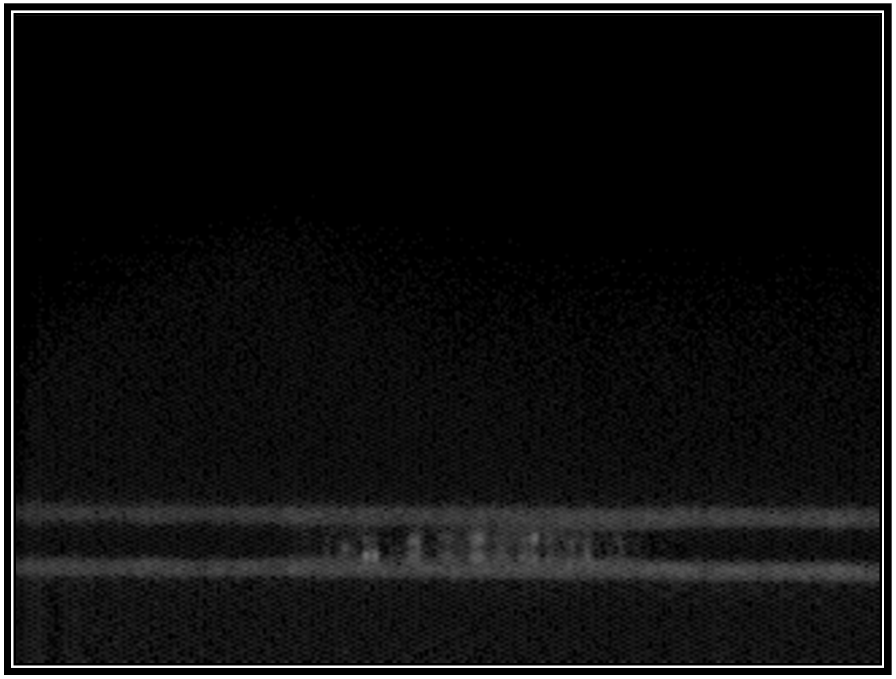
Conventional Stencil Technology

Manufacturing Processes	Concerns	Magnified image
Chemically etched	Isotropic etching produces Tapered sidewalls limiting pitch	
Laser Cut	Sequential process Laser-metal Interaction hence rough aperture sidewalls	
Electroformed	Aperture size and shape varies	

Stencil Release Performance

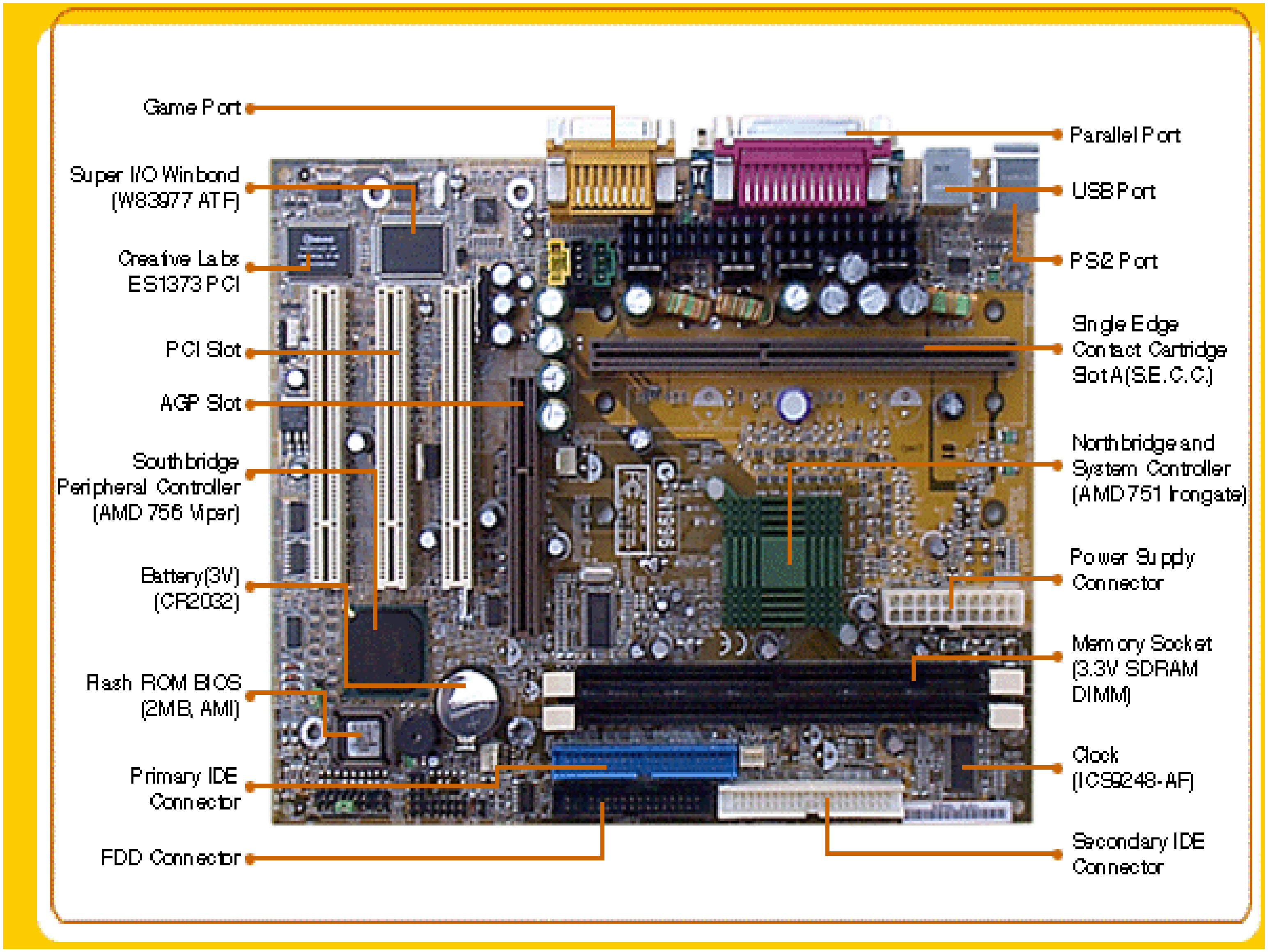


- **Laser Cut**
- Paste D
- 20 mil Aperture



- **ElectroFormed**
- Paste D
- 20 mil Aperture

Evaluating
Printed Circuit Board
Designs


Game Port
Super I/O Winbond (W83977 ATF)
Creative Labs ES1373 PCI
PCI Slot
AGP Slot
Southbridge Peripheral Controller (AMD 756 Viper)
Battery (3V) (CR2032)
Flash ROM BIOS (2MB, AMI)
Primary IDE Connector
FDD Connector
Parallel Port
USB Port
PS2 Port
Single Edge Contact Cartridge Slot A (S.E.C.C.)
Northbridge and System Controller (AMD 751 Irongate)
Power Supply Connector
Memory Socket (3.3V SDRAM DIMM)
Clock (ICS9248-AF)
Secondary IDE Connector

Classification of Electronic Assemblies

ANSI/J-STD-001 classifies three levels of electronic assemblies based on end-item use. The 3 classifications were established to reflect differences in producibility, complexity, functional performance requirements and verification frequency. They are as follows:

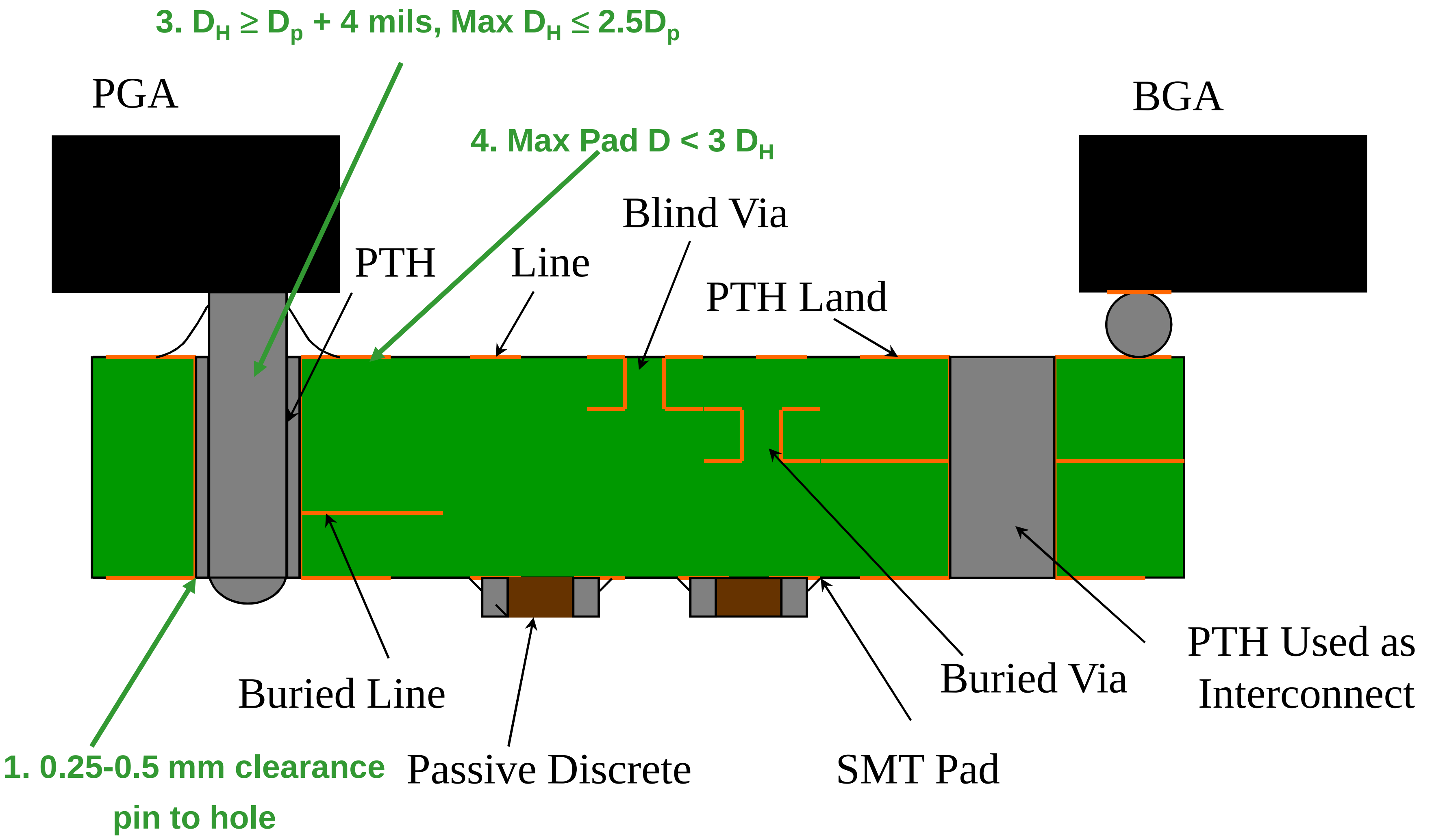
- **Class 1- General Electronic Products: Consumer products, computer and computer peripherals, and hardware suitable for applications where the major requirement is a function of the completed assembly**

(Source: Printed Circuits Handbook, pp 36.3, Coombs, ISBN: 0-07-012754-9)

Classification of Electronic Assemblies

- **Class 2**- Dedicated Service Electronic Products: Includes communication equipment, sophisticated business machines, and instruments where high performance and extended life are required, and for which uninterrupted service is desired but not critical
- **Class3**- High Performance Electronic Products: Includes equipment for commercial and military products where continued performance or performance on demand is critical

Standard Multi-Layer Interconnection



General Requirements

- PCB Should have good rigidity, minimal routing.
- PCB should have minimal warpage.
- Fiducials located on “Breakaways” of panelized boards may decrease accuracy.
- If aperture is not reduced, bridging and need for wiping will be increased.

Printed Circuit Board Size

- Maximum printed circuit board size (length, width, and thickness) determined by the particular process equipment being used.
- Minimum printed circuit board size (length, width, and thickness) determined by the particular process equipment being used.
- Boards smaller than the minimum size may be panelized (two or more individual circuits per panel).

Printed Circuit Board Size

- One factor that must be considered is the printed circuit board fabrication vendor’s material usage from a single process sheet. Significant savings can be obtained by increasing the number of boards that can be fabricated from a single process sheet.
- It is important to understand the printed circuit board supplier’s guidelines and preferences and adhere to them in designing the board. This is an excellent example of early supplier involvement.

Printed Circuit Board Shape

- Rectangular shaped boards with no cut outs or breakaways are always preferred.
- When breakaways are necessary, there are two common options;
  - The Route and Tab Method
  - The V Groove Method

Component Spacing

- There is no limit on maximum interpackage spacing
- Land to land spacing between adjacent components should be 1.25 mm clear space all around the edges of the printed board if boards are tested off the connector or 2.5 mm minimum if vacuum seal for testing is used.

Source: IPC-SM-782A, Section 3.6.1.1, pp 20

Component Spacing

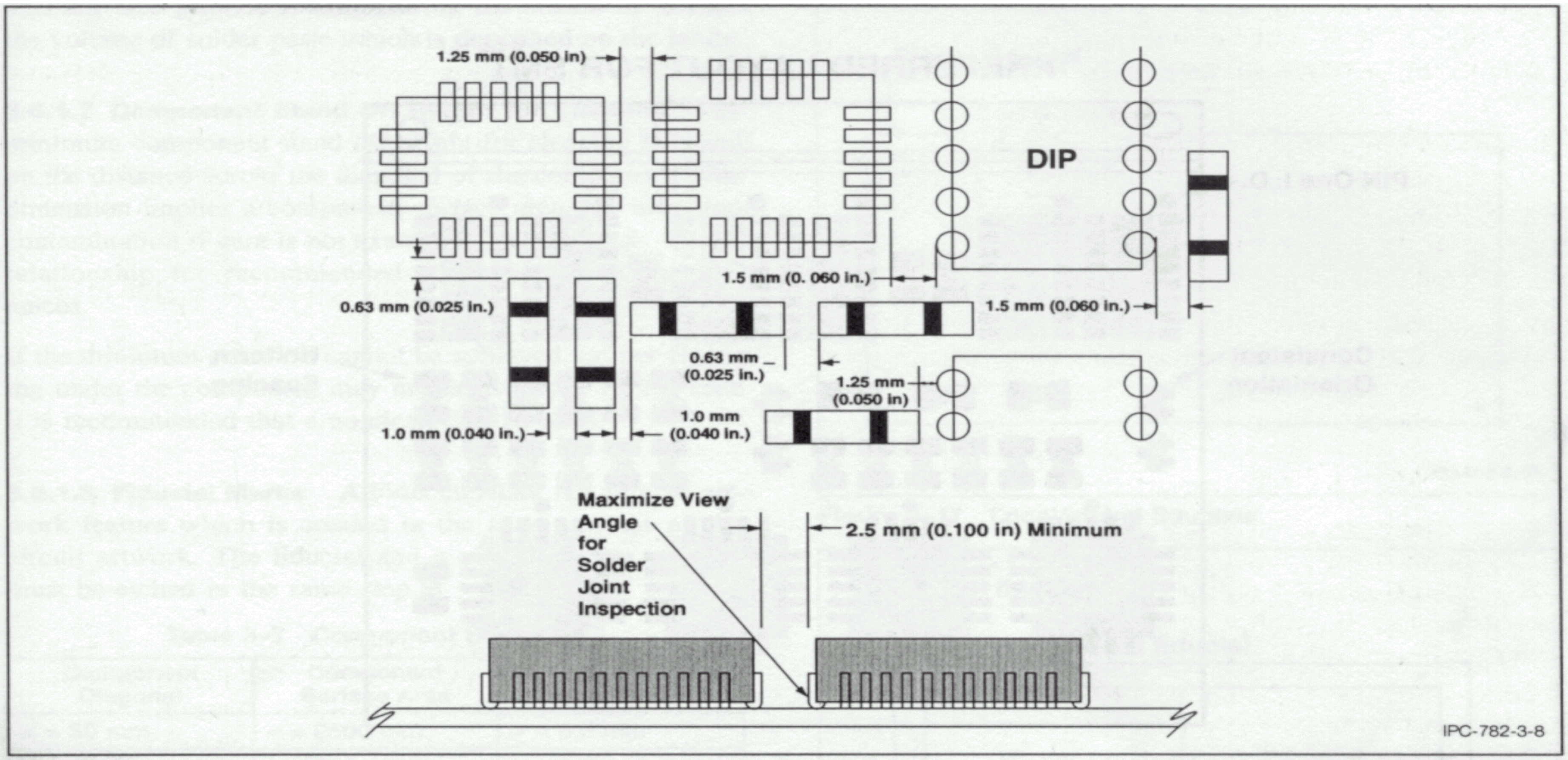


Figure 3–8 Recommended minimum land-to-land clearances

Source: IPC-SM-782A, page 21

Lead Protrusions

- For single sided PCB Assembly, lead or wire protrusion must be a minimum of 0.5 mm for all classes
- For double-sided and multilayer PCB Assembly, in all classes, the minimum lead protrusion is that the lead end be visible in the solder
- The maximum lead protrusion for Class 1 is that there should be no danger of shorts

Lead Protrusions

- For Class 2, the maximum lead protrusion is 2.5 mm and for Class 3 the maximum lead protrusion is 1.5 mm
- For boards thicker than 2.3 mm, the lead protrusions may not be visible

Source: Printed Circuits Handbook, pp 36.27

Edge Clearance Example

- No SMT components should be placed within 0.150” (3.81 mm) from the edges of a board.
- No traces or planes should be routed within 0.050” (1.27 mm) from the edge of a board.
- No via holes should be placed within 0.100” (2.54 mm) from the edge of a board.
- No test points (pads or via holes) should be placed within 0.125” (3.18 mm) from the edge of a board.

Component Hole Size

- Suppliers will have recommended hole sizes for specific components
- If a hole size is not recommended; use a hole that is .015” (.38 mm) larger than maximum lead diameter (round lead) or lead diagonal (square or rectangular lead).
- If the component is being automatically inserted, use the hole size recommended by the insertion equipment supplier.

Tooling Holes

- Required for location and fixturing of the boards during the fabrication, assembly and test processes.
- Requirements must be specified on a board outline drawing.
- Specific quantity, size, location, clearance, etc. will be determined by the Manufacturing/Process Engineer and specified in the printed circuit board design guidelines

Tooling Holes
Requirement Example

Quantity	4
Size (diameter)	0.159” +0.002” / - 0.001”
Location	4 corners
Plating	Non plated
Clearance (diameter)	0.25” from edge of hole
Datum	lower left corner hole

Fiducial Marks

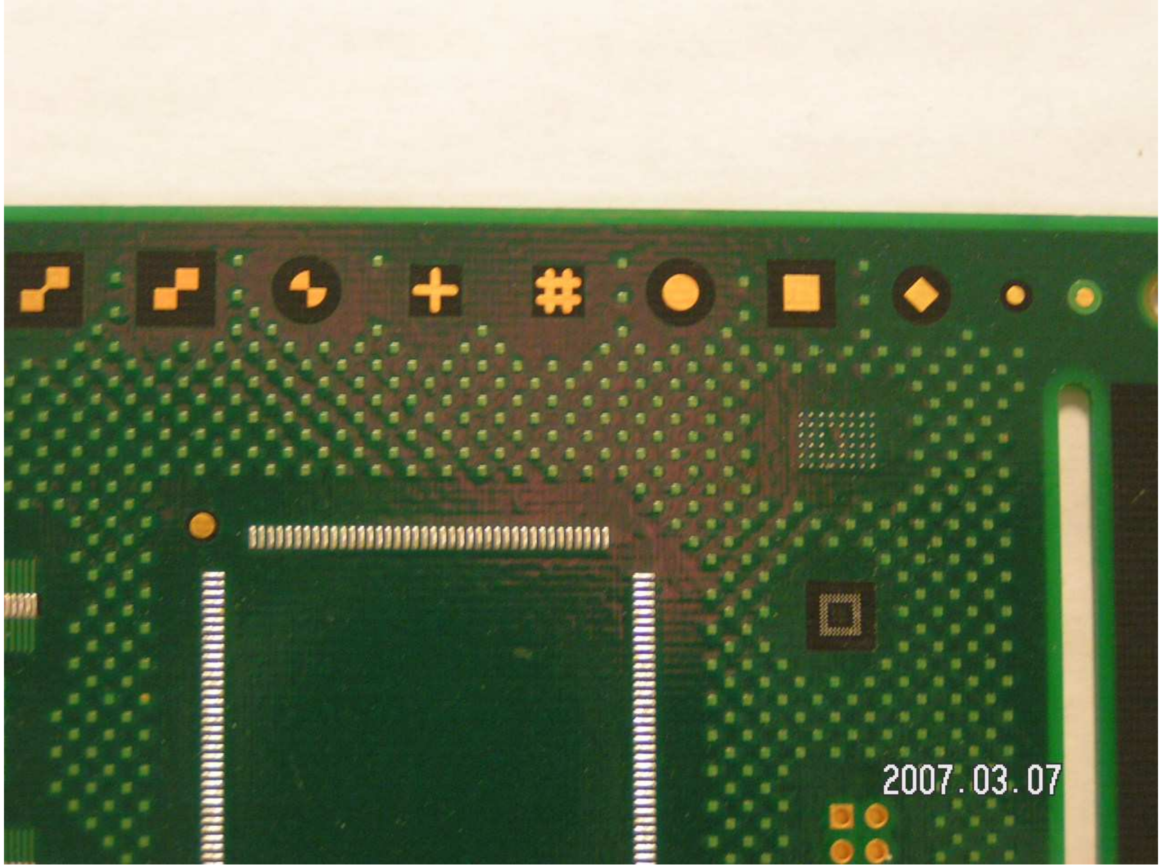
- Used by all automatic process equipment to precisely locate each printed circuit board.
- Two types of fiducial marks are used;
  - Board Level
  - Component Level
- Board level are used on every board to adjust the location of the stencil in the printer and to modify programs in the other process equipment.
- Component level are used on boards with complex components for very precise alignment.
- Exact shape and location determined by process

Board Level Fiducial Marks Example

- Quantity: 3 (minimum)
- Location: Corners of the board
- Size: .040” (1 mm) diameter pad
- Clearance: .120” (3 mm) diameter (no soldermask, traces, via holes, and legend/silk-screening)
- Edge Distance: .250” (6.35 mm) minimum

Board Level Fiducial Marks

A test board displaying a variety of fiducial mark geometries that can be used for stencil to board alignment



Courtesy or Speedline Technologies

Component Level Fiducial Marks Example

Component	Local Fiducial Required
BGA	No
.025” (.65 mm) pitch or greater	No
.020” (.5 mm) pitch less than 120 pins	No
.020” (.5 mm) pitch more than 120 pins	Yes
Less than .020” (.5 mm) pitch	Yes

Component Selection

- Always use existing components if possible
  - Reduce component variety
  - Reduce component cost
  - Reduce material storage and handling
  - Reduce feeder requirements
  - Minimize required feeder carriage space
  - Purchase larger component reels

Component Selection

- Maximize use of SMT components (ABC Costing)
- Minimize use of manually inserted components
- Consider through hole connectors if the “Pin in Paste Process” is used
- Use quality and cycle time data to influence component selection on new products
- Understand the impact on the process of new components prior to approving for design

Activity Based Costing

- Calculates the total cost of the assembly operation
  - Equipment
  - People
  - Overhead (lights, heat, etc.)
- Calculates number of components to be inserted
- Divides the total cost by the total components to determine the cost to assemble a component
- Automatically inserted components will have a much lower cost than manually inserted components
- Cost of assembly + material = product cost
- Some operations consider the cost of test

Slow Secondary Operations

- Avoid components that require slow secondary operations that are longer than the cycle time of the SMT manufacturing process and/or cannot be done in the in line process.
  - Undefill
  - Incapsulant
  - Hand soldering
  - Wire bonding
- Flip Chip, Chip on Board (COB), some Chip Scale Packages (CSP), TAB

Passive Use Growth

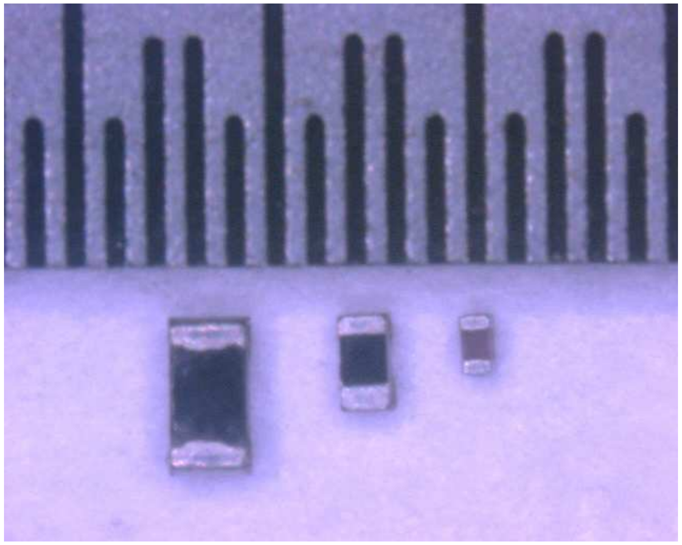
- A billion hours ago the stone age was the future
- A billion minutes ago Caesar ruled Rome
- A billion passives ago was this morning!
- Every year enough are produced to give each man, woman and child on the planet 160 passives

Size of 01005 Component

01005 Package Size = 10 mil (.010”) X 5 mil (.005”)

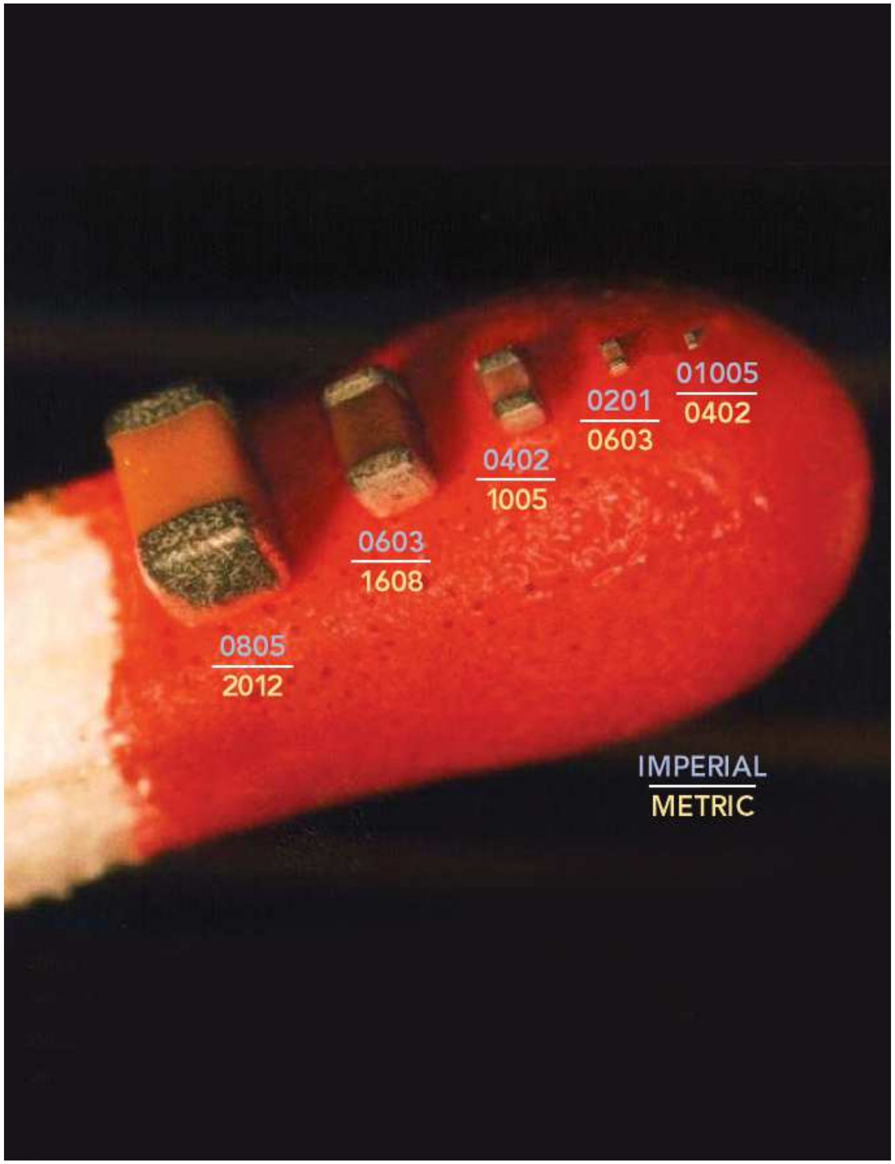
Or

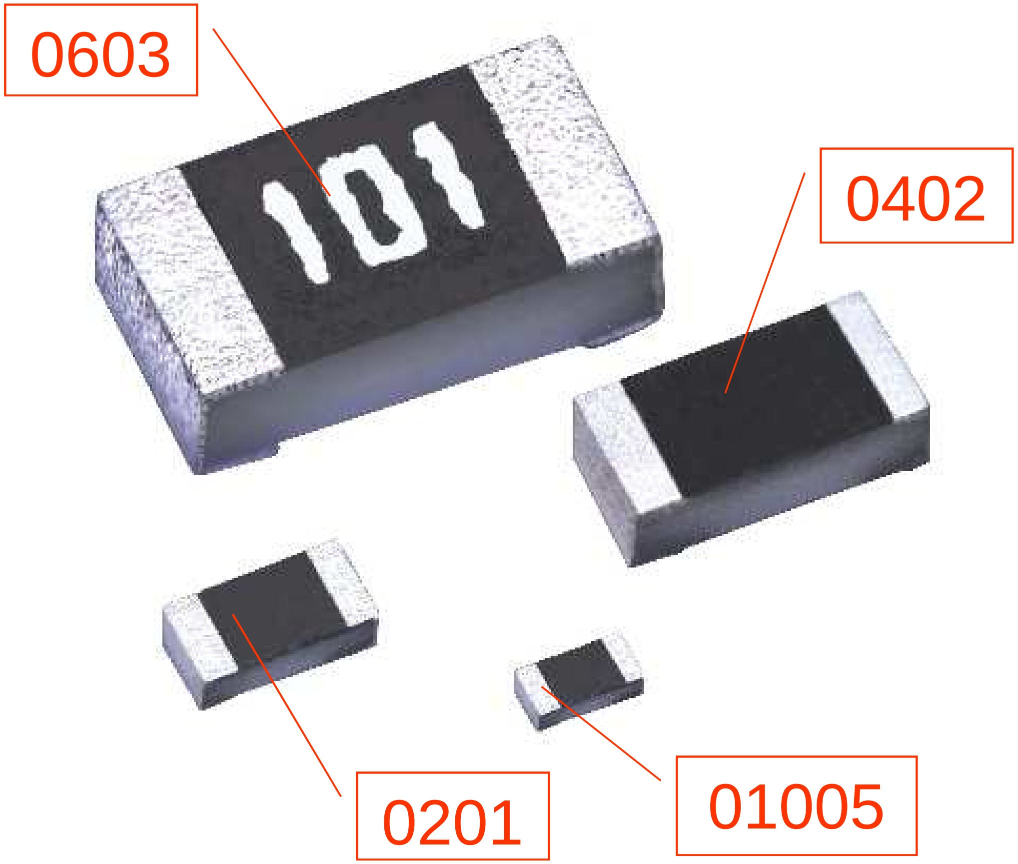
0.25 mm X 0.125 mm



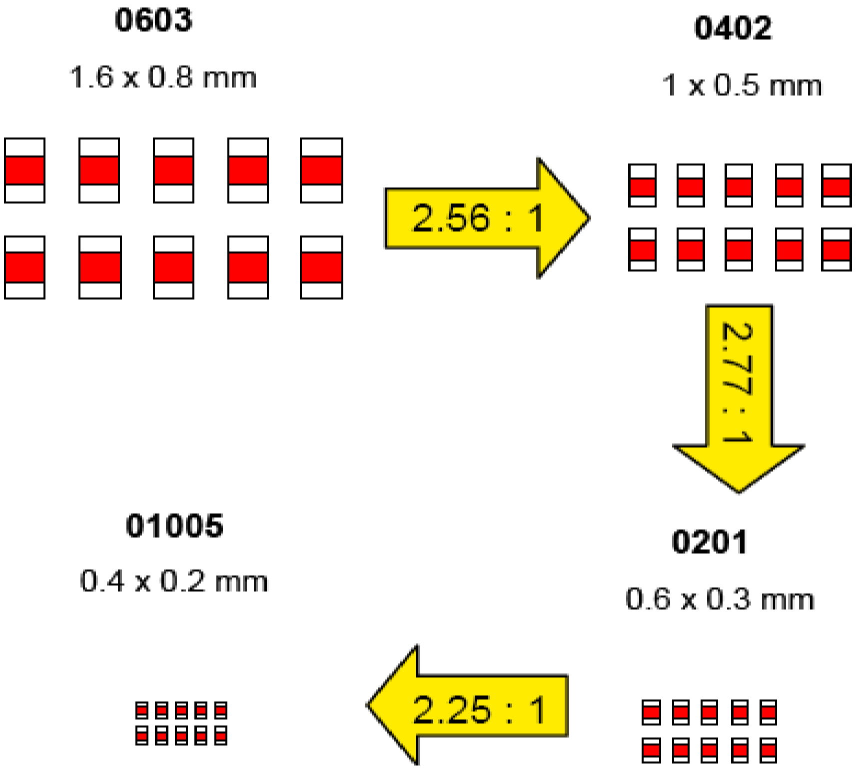
Their width (5 mils) is only slightly larger than the thickness of a human hair and their length about the thickness of a sheet of resume paper!

Imperial/Metric Component Sizes





Chip Component Size & Spacing Comparisons



0603

1.6 x 0.8 mm

2.56 : 1

0402

1 x 0.5 mm

2.77 : 1

0201

0.6 x 0.3 mm

2.25 : 1

01005

0.4 x 0.2 mm

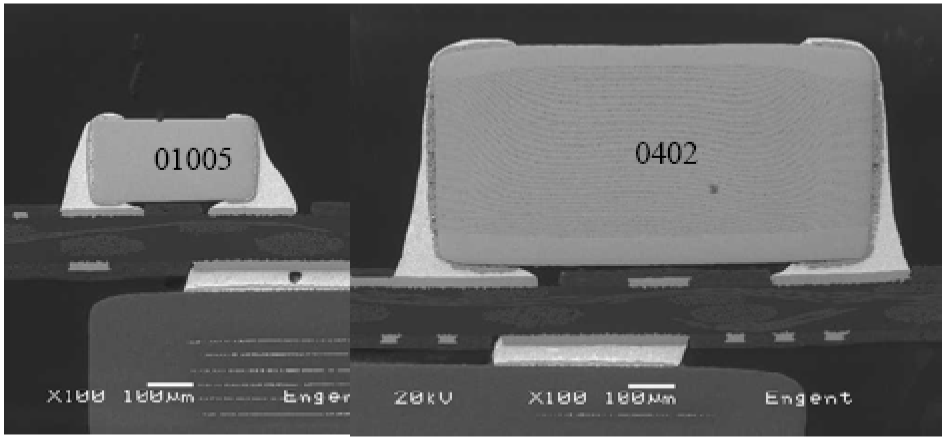
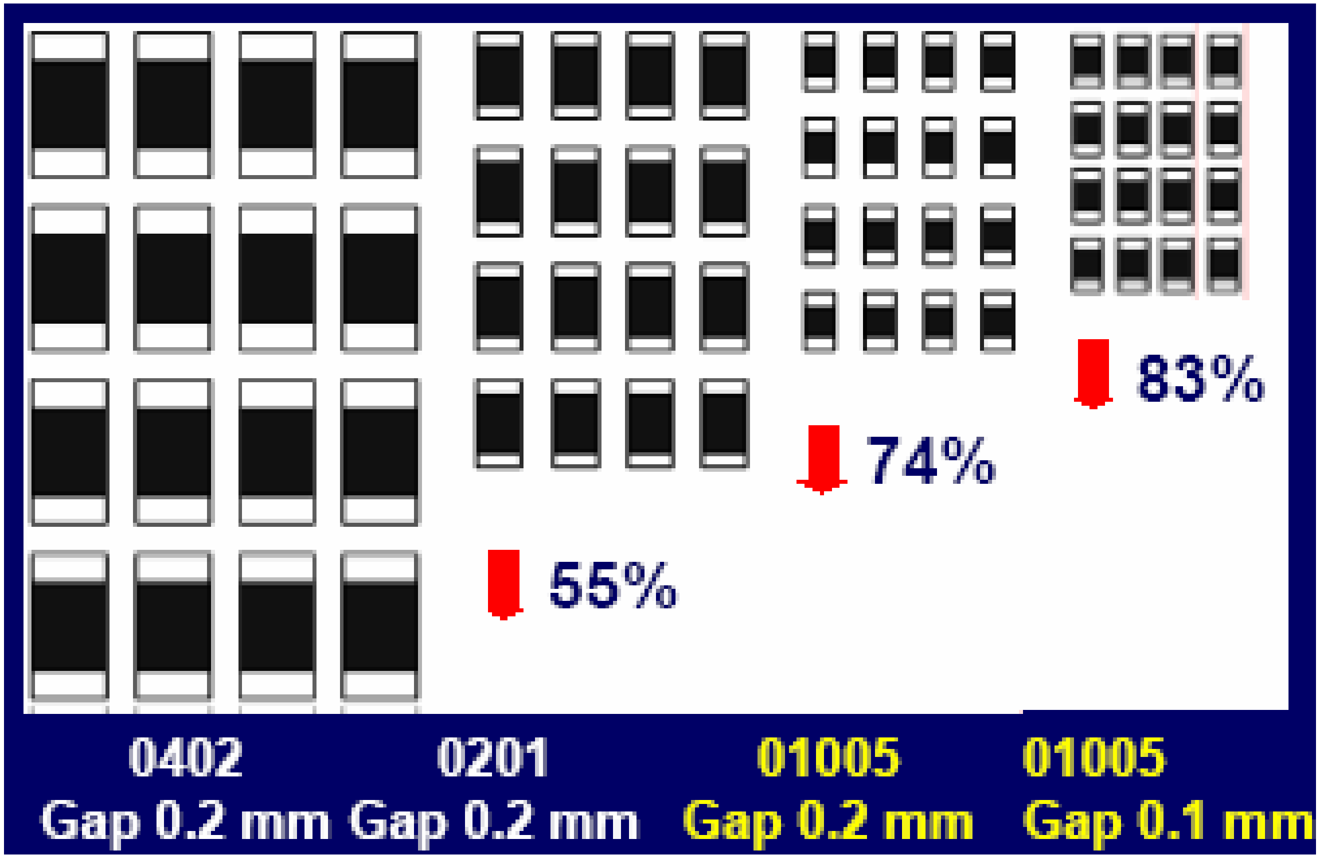


Figure 2: SEM Image of a 01005 at the Same Magnification as a 0402

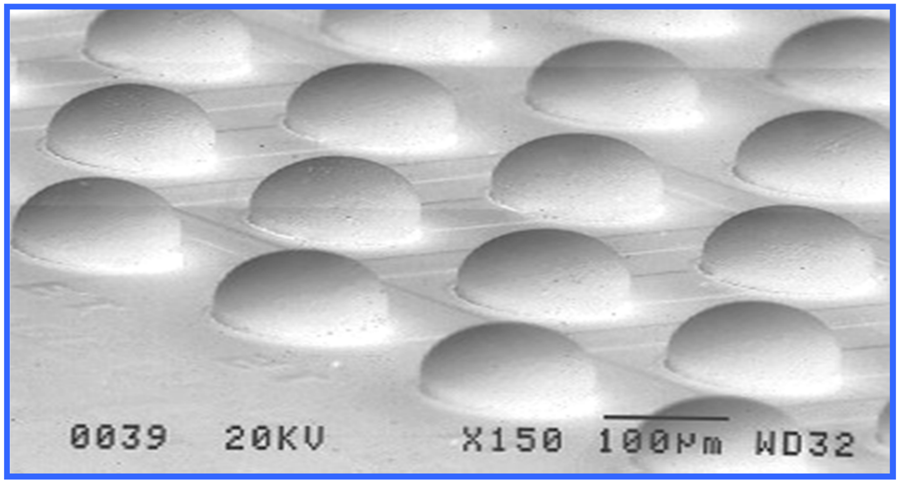
Houston et al; "Implementation of 01005's: a Case Study"; SMTAI-08

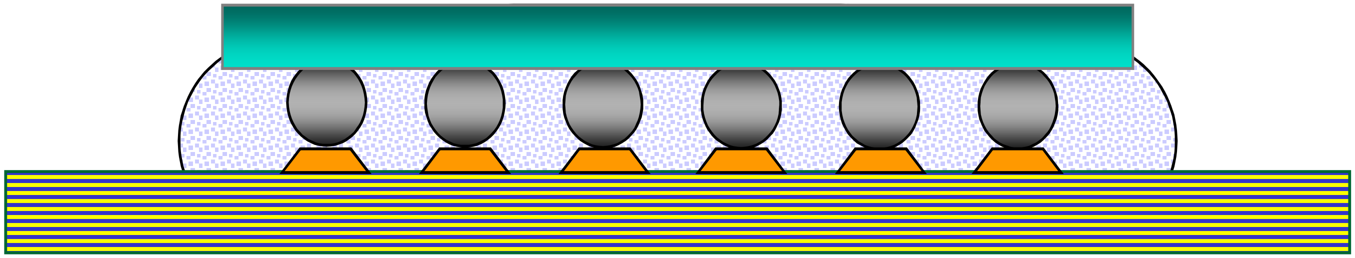
Chip Size and Spacing Options



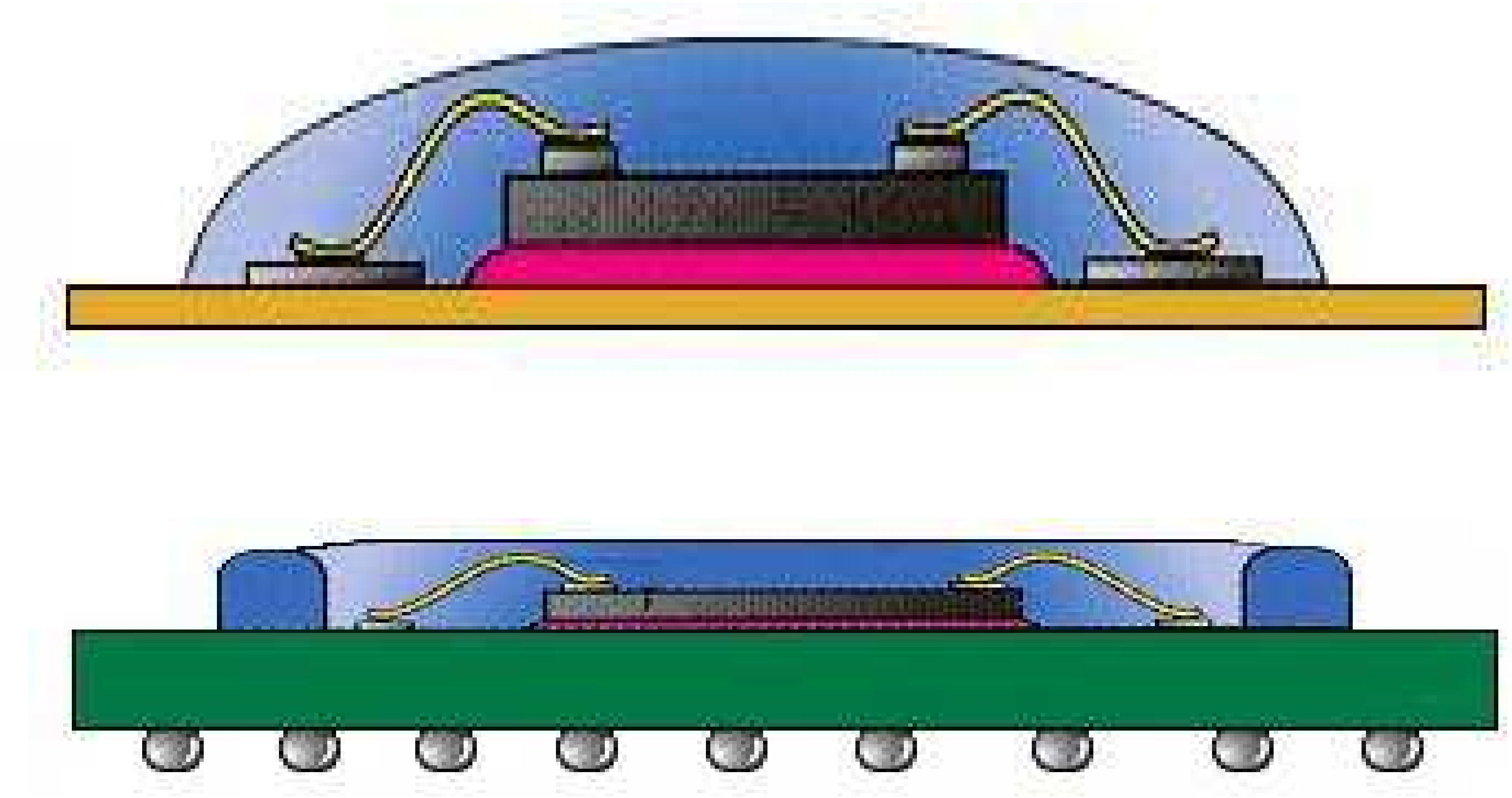
Chen, et al.; ASSEMBLY PROCESS RESEARCH ON 01005 CHIP COMPONENTS IN LEAD-FREE SYSTEM; SMTAI-06

Flip Chip

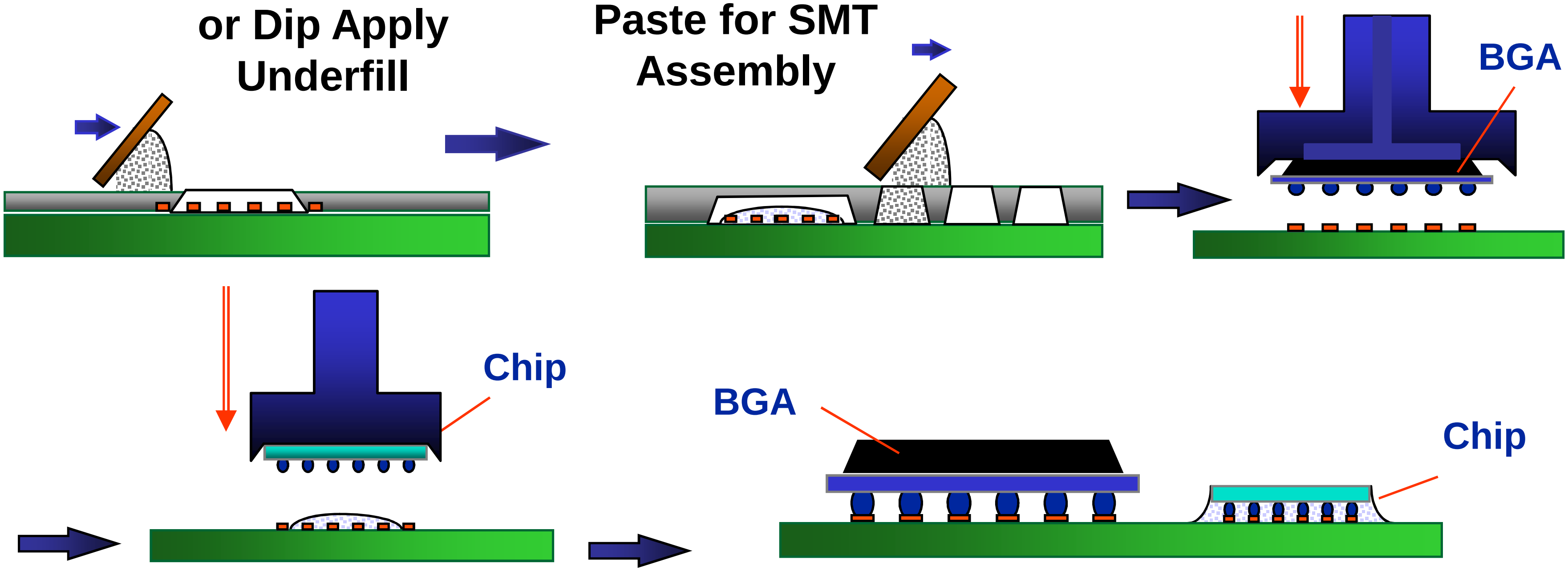




Chip on Board (COB)



FC = SMT Process



Print Underfill
or Dip Apply
Underfill

Print Solder
Paste for SMT
Assembly

Bare Chip Placement piercing
underfill to form partial fillets

Simultaneous
Solder Interconnect Reflow and
Underfill Cure

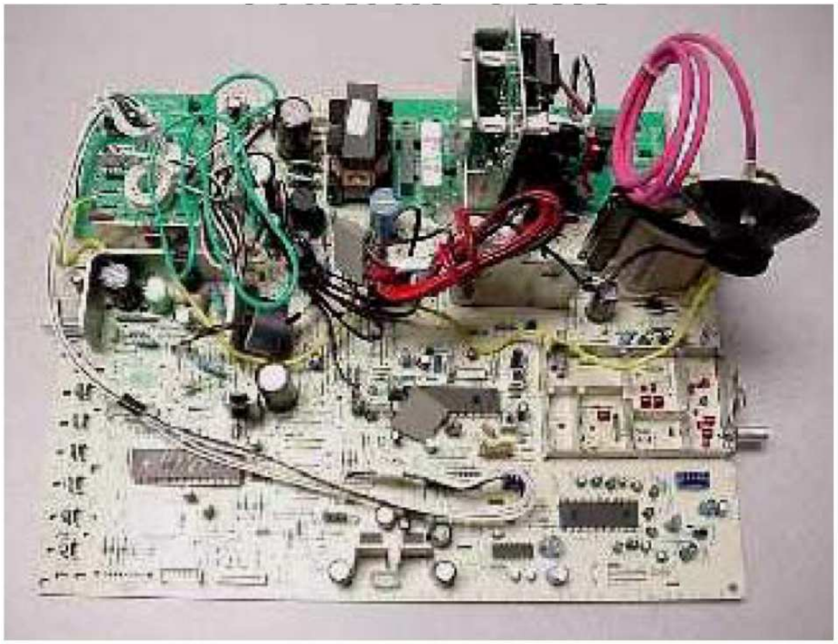
Component Placement

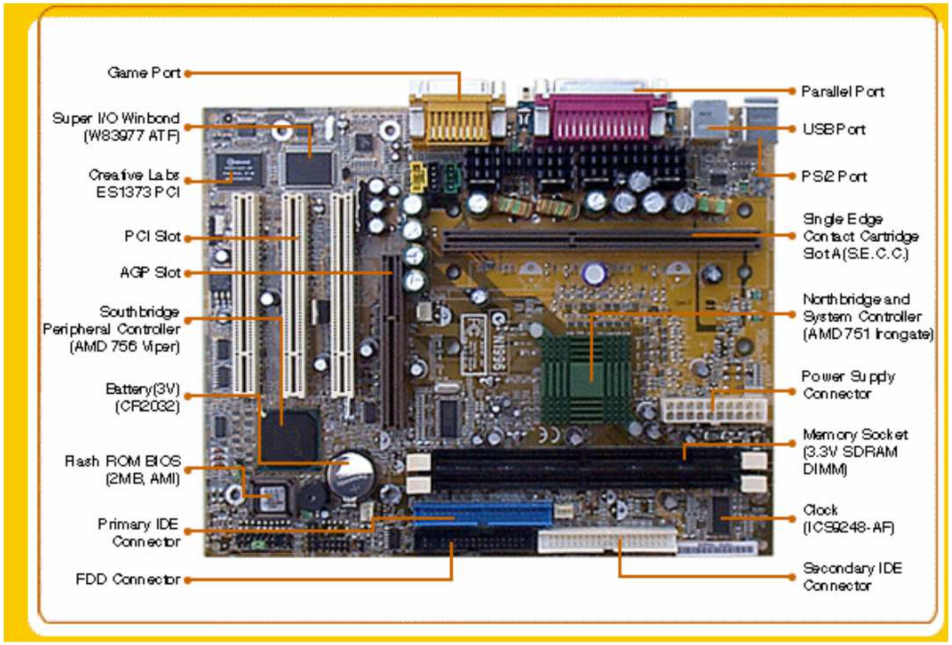
- The Printed Circuit Design Guidelines must specify the requirements for the placement of all components used (refer to PCB Design Guidelines for exact values).
  - Board side
  - Soldering process to be used
  - Spacing between components for reflow soldering
  - Spacing between components for wave soldering
  - Spacing between components and test points
  - Direction of travel through wave solder process
  - Size and location of solder thief pads for wave soldering

Component Footprints and Pads

- A library of component foot prints and pads is usually specified in the Printed Circuit Board Design Guidelines and maintained in the CAD System used to design the boards.
- There is an IPC Printed Circuit Board Design Specification (IPC781) that details component footprints and pad sizes.
- Reduce aperture size by 20% to your pad size, maintain a minimum of 1.5 aspect ratio of aperture width to stencil thickness. (.025”/.64 mm pitch and below).

Wave Soldering
Printed Circuit Board Design





Portions

Courtesy of:

Dale Lee
Dale.Lee@Guidant.com

Board Design Considerations for Wave Soldering

What Is Wave Soldering Yield Improvement Through Design?

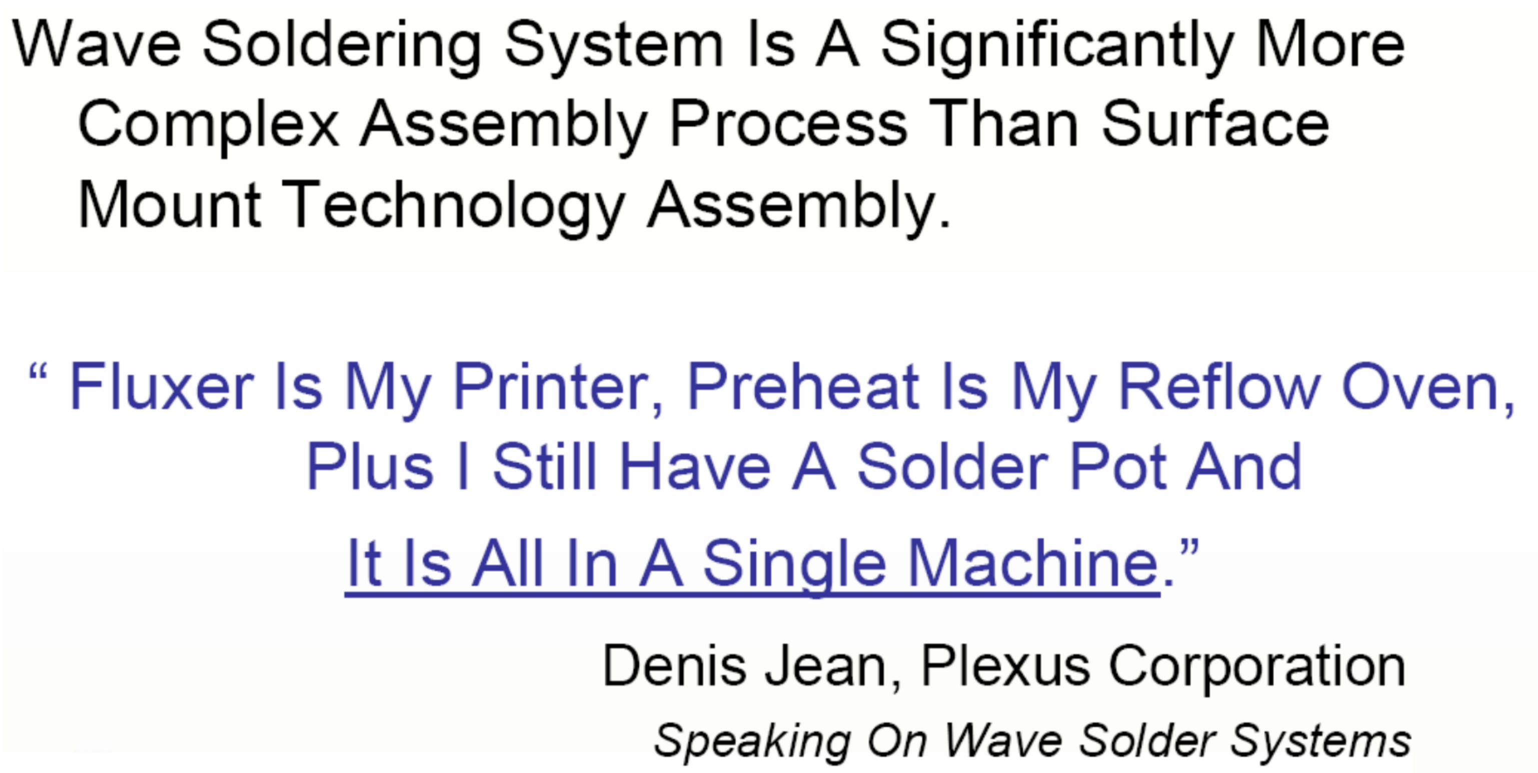
Impact Identification Of Design Elements On The Generation Of Electrical, Electromechanical And Mechanical Connections Through An Infinite Flowing Molten Metal Bath Precision Extraction Process For Printed Circuit Board Assembly

More Commonly Referred To As:

Wave Solder Design for Manufacturing

Board Design Considerations for Wave Soldering

SMT Versus Wave Soldering Process

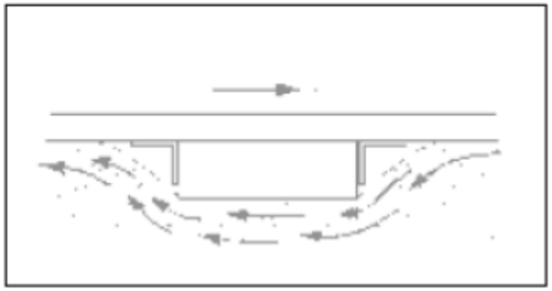


Wave Soldering System Is A Significantly More Complex Assembly Process Than Surface Mount Technology Assembly.

> " Fluxer Is My Printer, Preheat Is My Reflow Oven,
> Plus I Still Have A Solder Pot And
> It Is All In A Single Machine."

Denis Jean, Plexus Corporation
Speaking On Wave Solder Systems

Board Design Considerations for Wave Soldering



Factors that affect wave soldering yields:

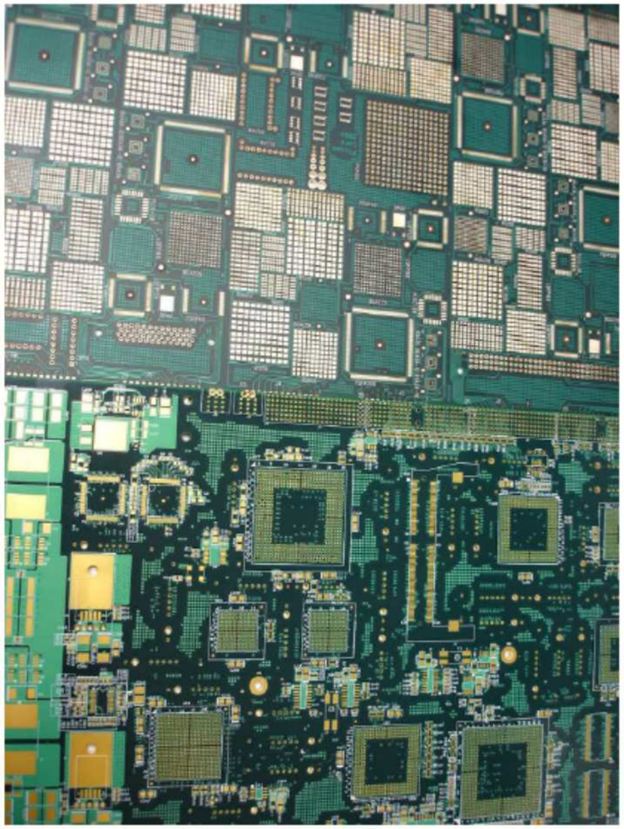
Number of Layers, Thickness of Copper, Thickness of Board, Amount of Exposed Solderable Surface, Assembly Orientation (Panelization), Component Placement Density Impacts Thermal Density, Preheating Capability and Solder Wetting

SMT & Thru-Hole Component Packaging, Pad Geometry and Orientation Impacts Solder Defect Generation

Solderability Impacted By PCB Surface Finish – Wetting and Solidification

Board Design Considerations for Wave Soldering

Preferred



Matte Finish Solder Mask Has Increase Surface Energy To Hold Flux To The Board (More Flux For Solder Joint Formation)

Dull/Low Reflection Appearance

Glossy Finish Solder Mask Has Low Surface Energy to Flux To The Board (Less Flux For Solder Joint Formation – Solder Balls, Icicles, Flags, etc.)

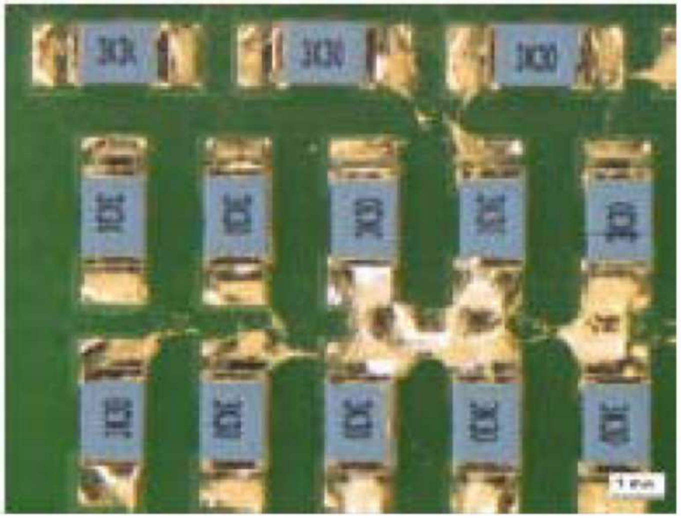
Highly Reflective Appearance

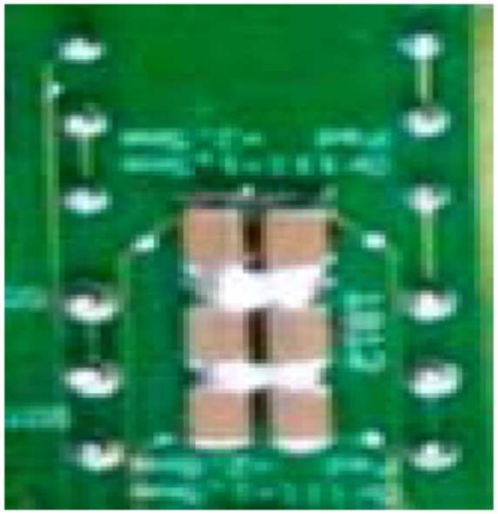
Not Preferred

Board Design Considerations for Wave Soldering

Solder Mask Selection Impact

- A Low Surface Energy Glossy Finish Can Generate Solder Defects Similar In Appearance To No Flux Or Too Little Flux On The Board.
- Resulting in Whiskers, Strings, Peaks, Bridges, Icicles, Solder Balls, Solder Web, Solder Flags



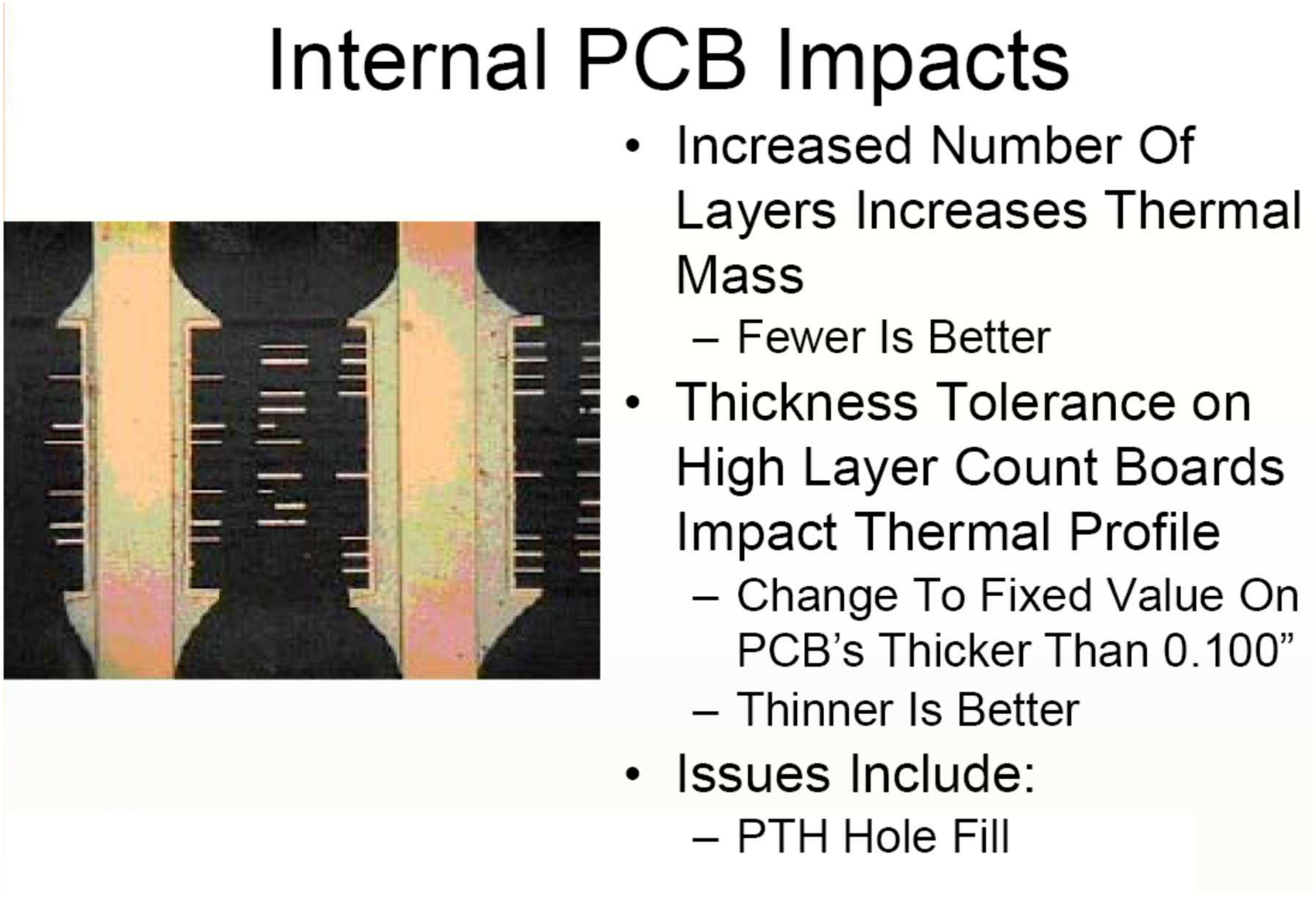


Board Design Considerations for Wave Soldering

- The ratio of the size of a printed board hole to the diameter of a through-hole lead
- The distance of solder joints from the edge of a printed board
- The distance from a component body to the edge of a printed board

Source: IPC-AJ-820, Section 8.3.7, pp 8-15

Board Design Considerations for Wave Soldering

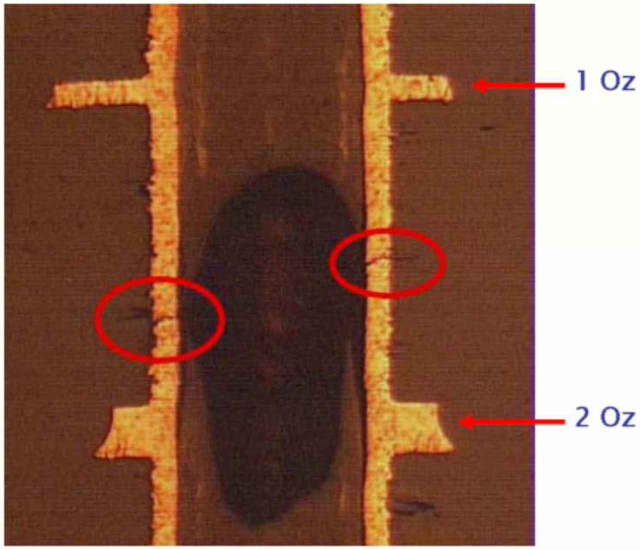


Internal PCB Impacts

- Increased Number Of Layers Increases Thermal Mass
  - Fewer Is Better
- Thickness Tolerance on High Layer Count Boards Impact Thermal Profile
  - Change To Fixed Value On PCB's Thicker Than 0.100"
  - Thinner Is Better
- Issues Include:
  - PTH Hole Fill

Board Design Considerations for Wave Soldering

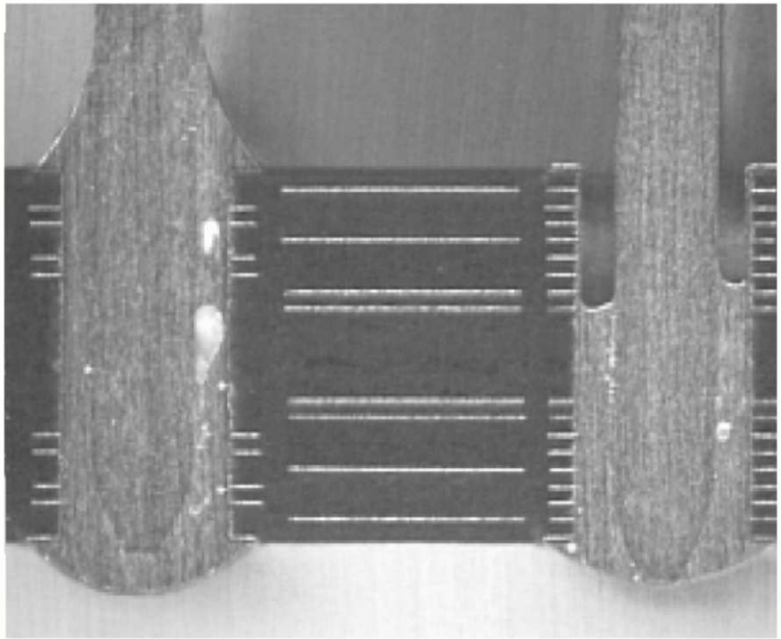
Internal PCB Impacts



- Copper Plane
  - Uniform Thickness
  - Balanced Thickness To PCB Centerline
- Thicker Copper Plane Layers Increase Thermal Mass
  - Thinner Is Better
  - Increase Thermal Pad Isolation
- Issues Include:
  - PCB Warping
  - PTH Hole Fill

Board Design Considerations for Wave Soldering

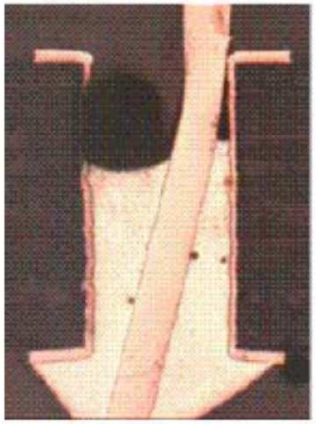
Internal PCB Impacts



- **Number Of Layer Connections to Plated Through Hole**
  - **Increased Number Of Layer Connections Increases Thermal Mass Of Plated Through Hole**
  - **Increased Number Of Plane Layer Connections Greatly Increases Thermal Mass Of Plated Through Hole**
- **Issues Include:**
  - **PTH Hole Fill**

Board Design Considerations for Wave Soldering

What To Do?



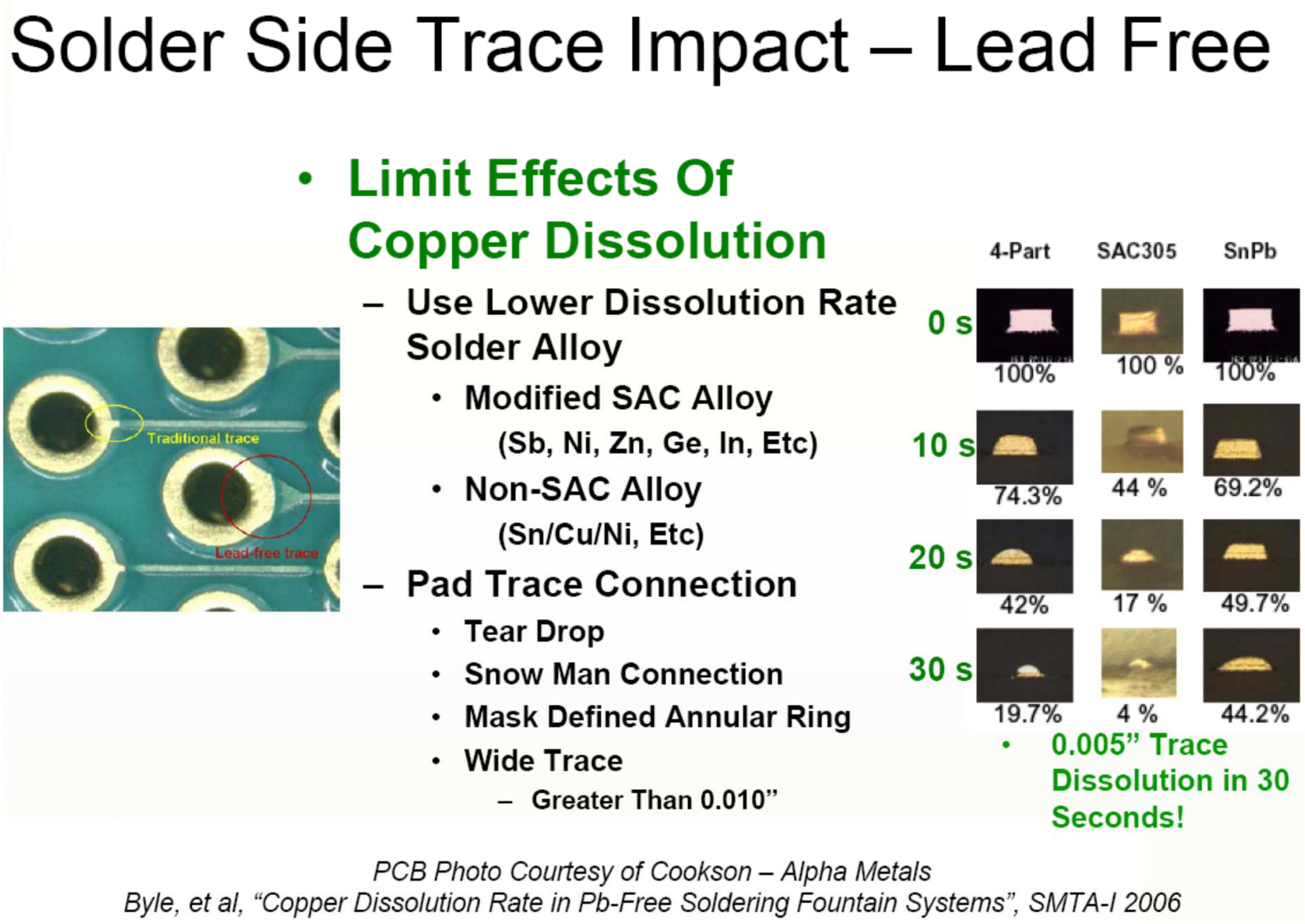
250°C

Increase Solder Temperature?

Lead Free Solder Issue

- **Higher Solder Temperatures Or Increased Solder Dwell Times Create Problems With Pads On Solder Side**

Board Design Considerations for Wave Soldering



Solder Side Trace Impact – Lead Free

- **Limit Effects Of Copper Dissolution**
  - Use Lower Dissolution Rate Solder Alloy
    - Modified SAC Alloy
      (Sb, Ni, Zn, Ge, In, Etc)
    - Non-SAC Alloy
      (Sn/Cu/Ni, Etc)
  - Pad Trace Connection
    - Tear Drop
    - Snow Man Connection
    - Mask Defined Annular Ring
    - Wide Trace
      - Greater Than 0.010”

	4-Part	SAC305	SnPb
0 s	100%	100 %	100%
10 s	74.3%	44 %	69.2%
20 s	42%	17 %	49.7%
30 s	19.7%	4 %	44.2%

- 0.005” Trace Dissolution in 30 Seconds!

PCB Photo Courtesy of Cookson – Alpha Metals

Byle, et al, “Copper Dissolution Rate in Pb-Free Soldering Fountain Systems”, SMTA-I 2006

Board Design Considerations for Wave Soldering

- The rigidity of the base material at the elevated soldering temperature
- The degree of retention that is used to prevent component movement during soldering
- The degree to which solder resist marks and legend marking are used with respect to not having them bleed onto surfaces that are to be soldered

Source: IPC-AJ-820, Section 8.3.7, pp 8-15

Board Design Considerations for Wave Soldering

- The thermal loading of the printed board
- The relieving of large metal planes, such as ground planes, in order to minimize “heat sinking” effects.
- The configuration of lands

Source: IPC-AJ-820, Section 8.3.7, pp 8-15

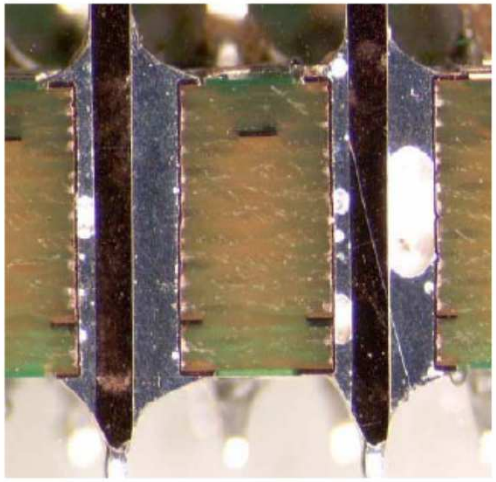
Lead Configuration for Through-Hole Assembly

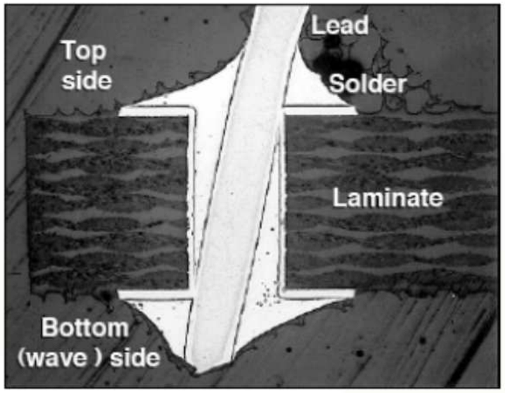
1. Generally 0.25 to 0.5 mm clearance between Lead to Hole is used (Source: IPC-AJ-820, Section 2)
2. The hole size should be no less than lead diameter plus 4 mils and the maximum hole diameter should be no more than 2.5 times the lead diameter (Source: Printed Circuits Handbook, pp 28.3, Coombs, ISBN: 0-07-012754-9)
3. The pad area around the solder joint is usually circular and should be no more than 3 times the diameter of the hole in the board (Source: Printed Circuits Handbook, pp 28.3,Coombs, ISBN: 0-07-012754-9)
    - Pad Dia = 3 x pin dia is common **(Source: "Soldering Handbook for Printed Circuits and Surface Mounting", Manko, H., ISBN:013-823055-2)**
4. The lead if clinched should not extend beyond the edge of the land (Source: IPC-AJ-820, Section 2)

Lead to Hole Clearance

Lead To Hole Clearance

- Tin/Lead Solder
  - – Typical Lead To Hole Clearance Must Provide Adequate Space For Flux & Solder To Flow For Top Side Fillet Formation
    - Pin Size + 0.012” (Preferred)
    - Pin Size + 0.008” (Minimum Acceptable)
  - – Increasing Board Thickness May Increase Lead To Hole Clearance (Aspect Ratio)
- Lead Angle In Hole Combined With Lead Clearance Can Impact Void Creation In Plated Through Hole.
  - – Lead Type Can Impact Void Creation
    - Round Versus Flat Ribbon





Lead to Hole Clearance

Lead To Hole Clearance – Lead Free

- **Lead Free Soldering**
  - Lead Clearance Minimum Will Increase
    - Pin Size + 0.015" (Preferred)
    - Pin Size + 0.010" (Minimum Acceptable)
  - Increasing Board Thickness May Increase Lead To Hole Clearance (Aspect Ratio)
  - Larger Holes Create Less Voids
- **Smaller Hole To Lead Clearance Decreases Shrinkage Holes / Hot Tear Joints**

Plated-Through Hole/Component Hole Lands

The size and shape of all through hole lands and their annular rings should be maximized wherever feasible

Worst Case land to Hole relationship is given below

Land Size, minimum: $L_{min} = a + 2b + c$, where,

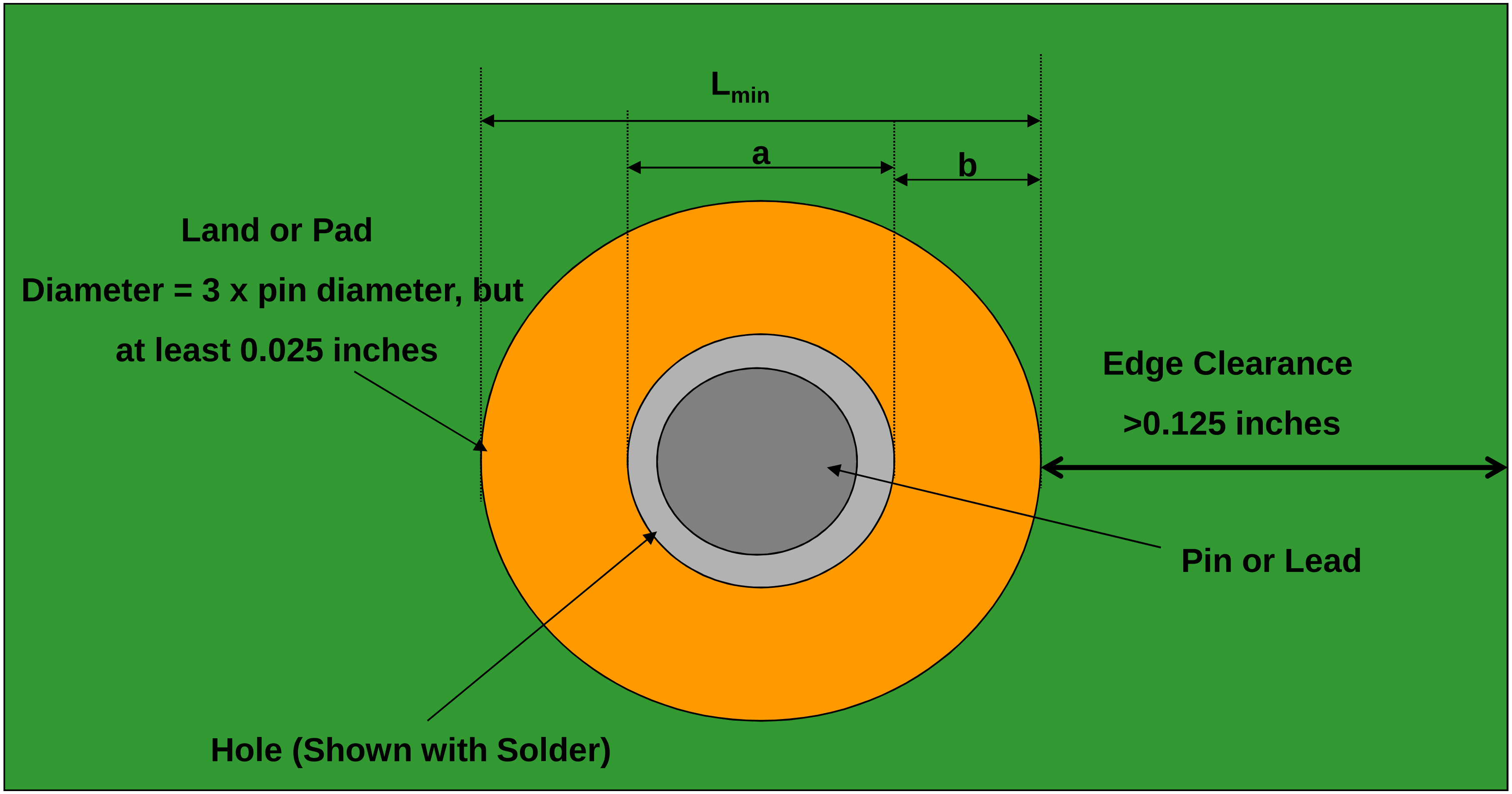
a = Maximum diameter of the finished hole

b = Minimum annular ring requirements

c = A standard fabrication allowance

Source IPC-D-330, Section 6, pp 45

Plated-Through Hole/Component Hole Lands



Land or Pad

Diameter = 3 x pin diameter, but

at least 0.025 inches

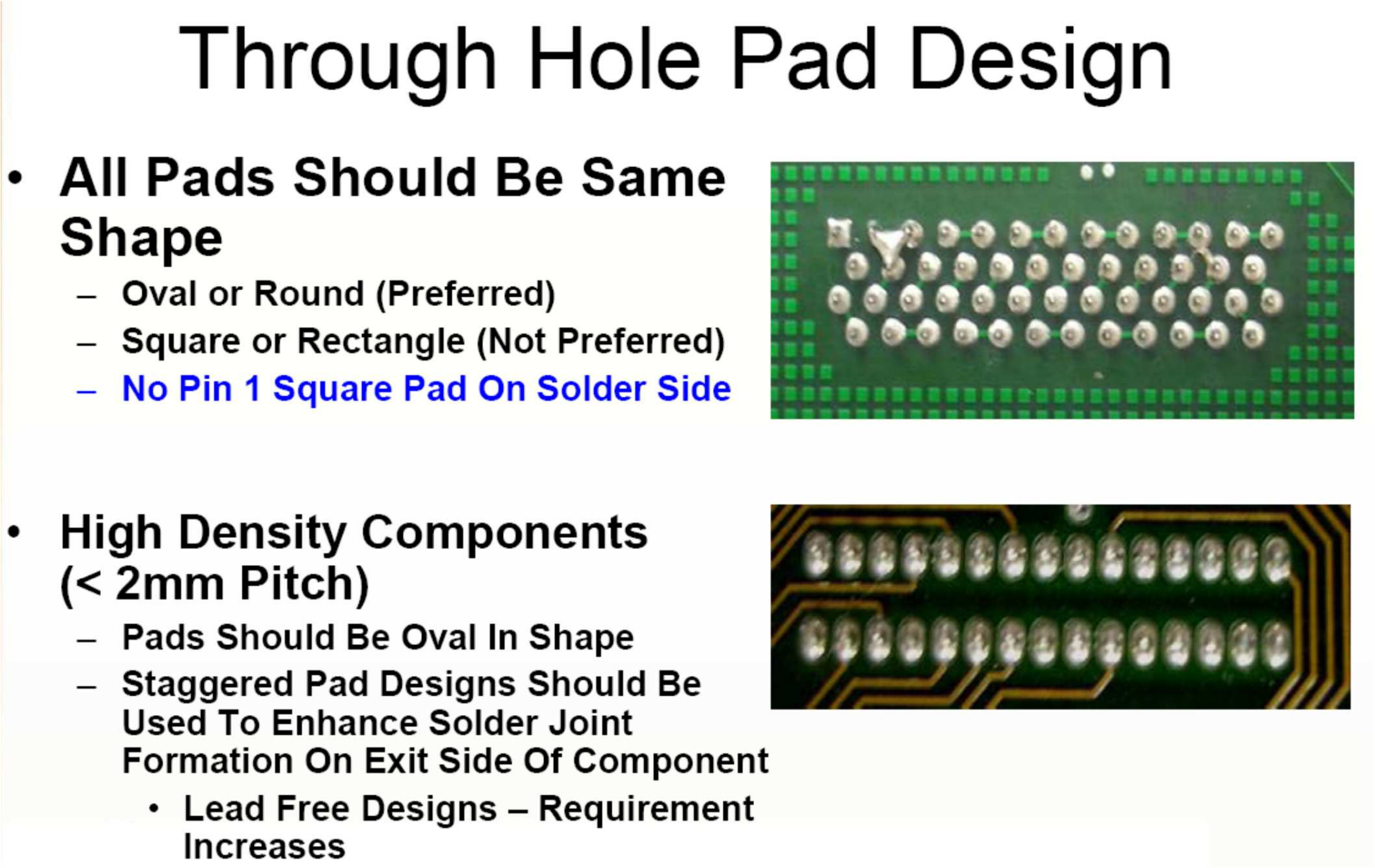
Edge Clearance

>0.125 inches

Pin or Lead

Hole (Shown with Solder)

Plated-Through Hole/Component Hole Lands



Through Hole Pad Design

- **All Pads Should Be Same Shape**
  - Oval or Round (Preferred)
  - Square or Rectangle (Not Preferred)
  - No Pin 1 Square Pad On Solder Side
- **High Density Components (< 2mm Pitch)**
  - Pads Should Be Oval In Shape
  - Staggered Pad Designs Should Be Used To Enhance Solder Joint Formation On Exit Side Of Component
    - Lead Free Designs – Requirement Increases

Plated-Through Hole/Component Hole Lands

Through Hole Pad Design – Lead Free

Square Pads Should Not Be Used On Solder Side

- Increased Solder Defect – Bridge/Flag/Web
- Increased Pad Lifting*

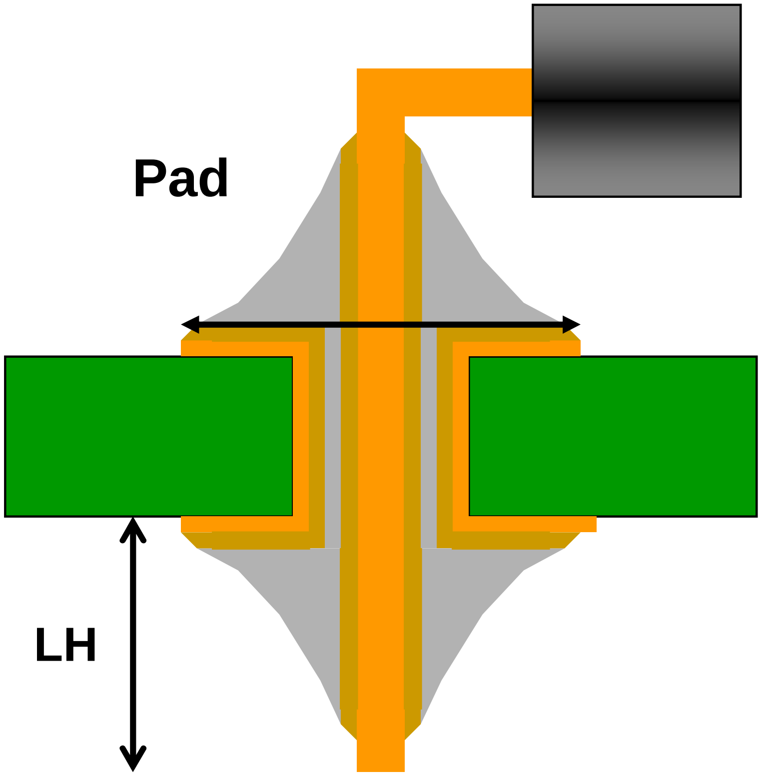
Decrease Component / Top Side Pad Size**

- Reduced Fillet Lifting

** Dr. S. Zweiger, Solectron GMBH, Productronica Green Day, November 2005*

*** K Puttlitz, K Stalter, "Handbook of Lead-Free Solder Technology For Microelectronic Assembly", pp 628, Fig 48*

Lead Height to Pad Ratio



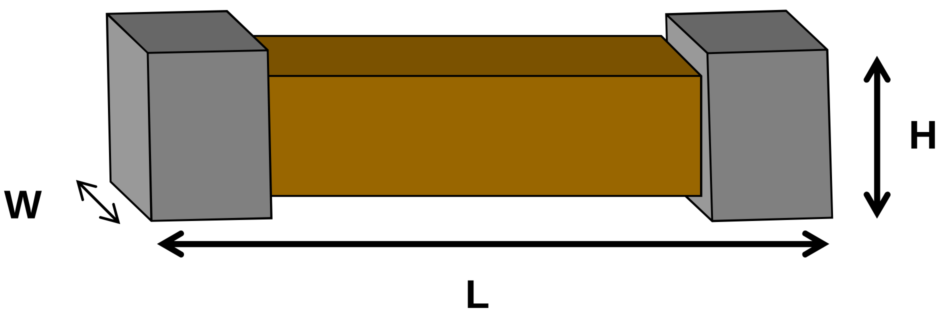
LH/Pad Diameter = 1.1 to 1.2

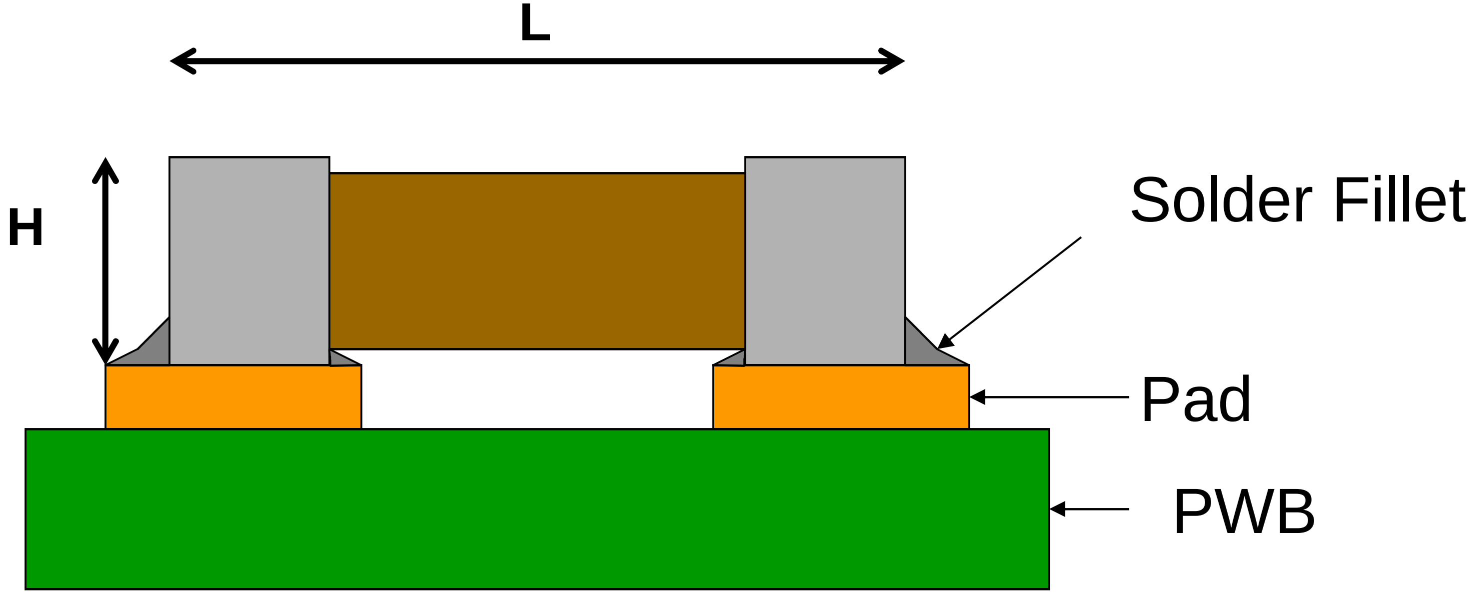
Plated-Through Hole/Component Hole Lands

- Sound joints are obtained with a ratio of 1:1 to 1:2 between lead height and pad width
- Clearance of 0.125 in along the long edges of the board

(Source: “Soldering Handbook for Printed Circuits and Surface Mounting”, Manko, H., ISBN:013-823055-2)

Passive Dimensions





Basic SMT Land Pattern Criteria

Following is a common land size design guideline for both Reflow and Wave soldered assemblies for resistors

Land Width (X) = $W_{max} - K$

Land Length (Y) = $H_{max} + K$

Gap (A) = $L_{max} - 2T - K$

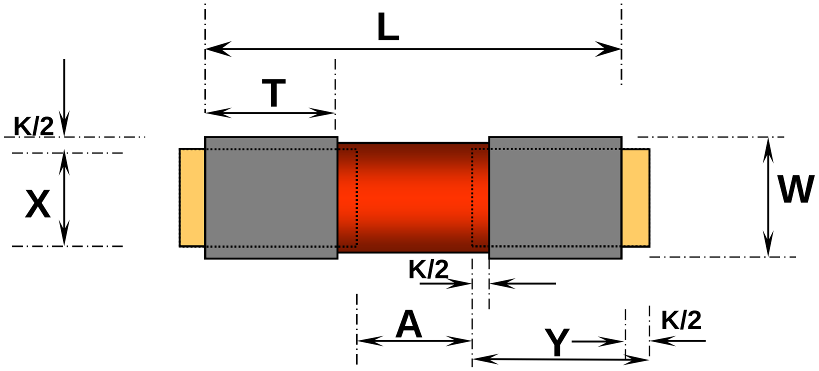
where:

W = Component Width L= Component Length

H= Component Height T= Solderable termination width

K= 0.25 mm

(Source: IPC-D-330, Section 11, pp 51)



SMT Land Pattern Criteria

Through Hole Pad Design – Lead Free

Square Pads Should Not Be Used On Solder Side

- Increased Solder Defect – Bridge/Flag/Web
- Increased Pad Lifting*

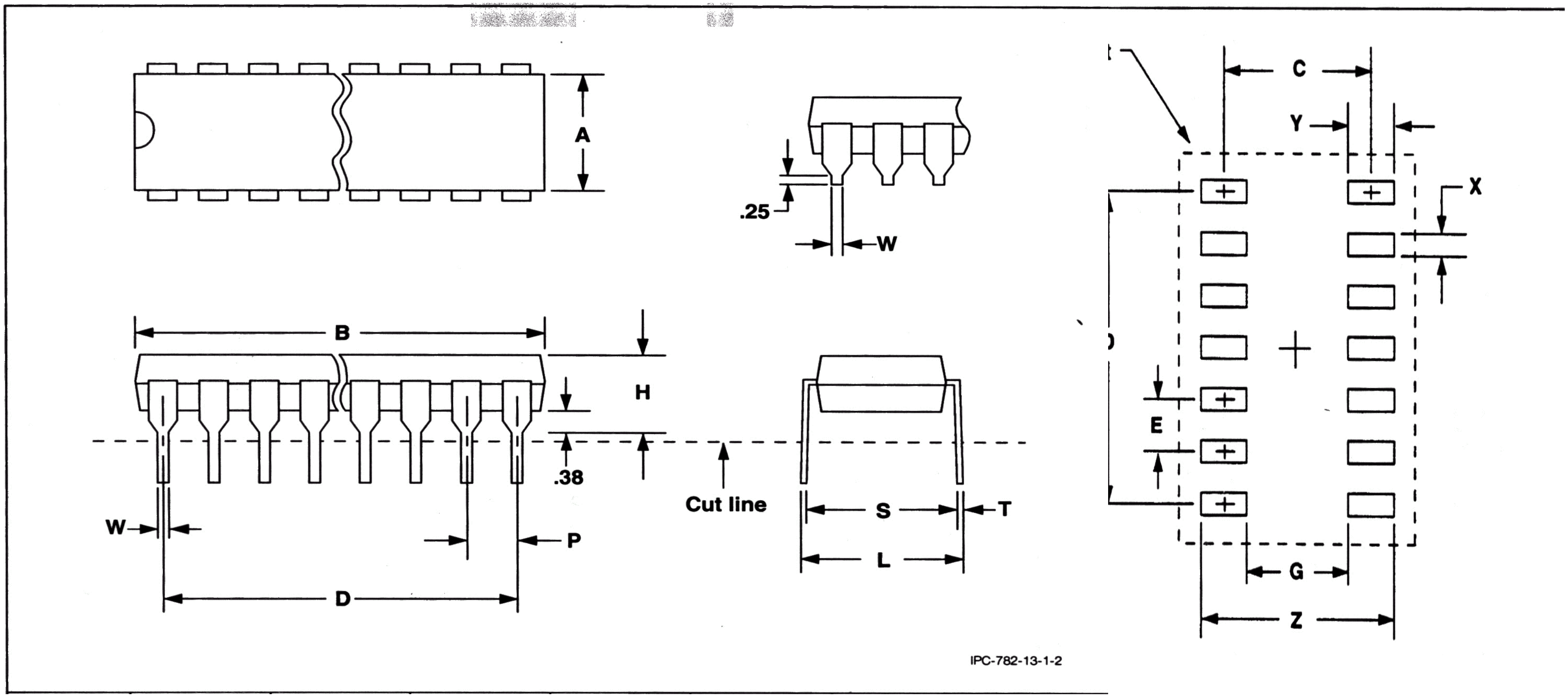
Decrease Component / Top Side Pad Size**

- Reduced Fillet Lifting

* Dr. S. Zweiger, Solectron GMBH, Productronica Green Day, November 2005

** K Puttlitz, K Stalter, "Handbook of Lead-Free Solder Technology For Microelectronic Assembly", pp 628, Fig 48

Component & Land Dimensions for a DIP



Source: IPC-SM-782, Section 13.1,

Component & Land Dimensions for a DIP

DIP Component Dimensions

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	max	basic
DIP 8	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	8.84	10.92	5.33	2.54
DIP 14	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	18.42	20.19	5.33	2.54
DIP 16	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	18.93	21.33	5.33	2.54
DIP 18	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	21.47	23.49	5.33	2.54
DIP 20	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	23.5	26.9	5.33	2.54
DIP 22L	9.91	10.79	9.15	10.07	0.36	0.56	0.2	0.38	8.39	9.65	26.67	28.44	5.33	2.54
DIP 24	7.62	8.25	6.86	7.54	0.36	0.56	0.2	0.38	6.1	7.11	28.6	32.3	5.33	2.54
DIP 24L	9.91	10.79	9.15	10.07	0.36	0.56	0.2	0.38	8.39	9.65	29.21	30.98	5.33	2.54

DIP Land Pattern Dimensions

RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
860	**DIP 8**	9.8	5.4	1.2	2.2	7.6	7.62	2.54	**22x24**
861	**DIP 14**	9.8	5.4	1.2	2.2	7.6	15.24	2.54	**22x42**
862	**DIP 16**	9.8	5.4	1.2	2.2	7.6	17.78	2.54	**22x44**
863	**DIP 18**	9.8	5.4	1.2	2.2	7.6	20.32	2.54	**22x48**
864	**DIP 20**	9.8	5.4	1.2	2.2	7.6	22.86	2.54	**22x56**
865	**DIP 22L**	12.4	8	1.2	2.2	10.2	25.4	2.54	**26x58**
866	**DIP 24**	9.8	5.4	1.2	2.2	7.6	27.94	2.54	**38x66**
867	**DIP 24L**	12.4	8	1.2	2.2	10.2	27.94	2.54	**26x64**

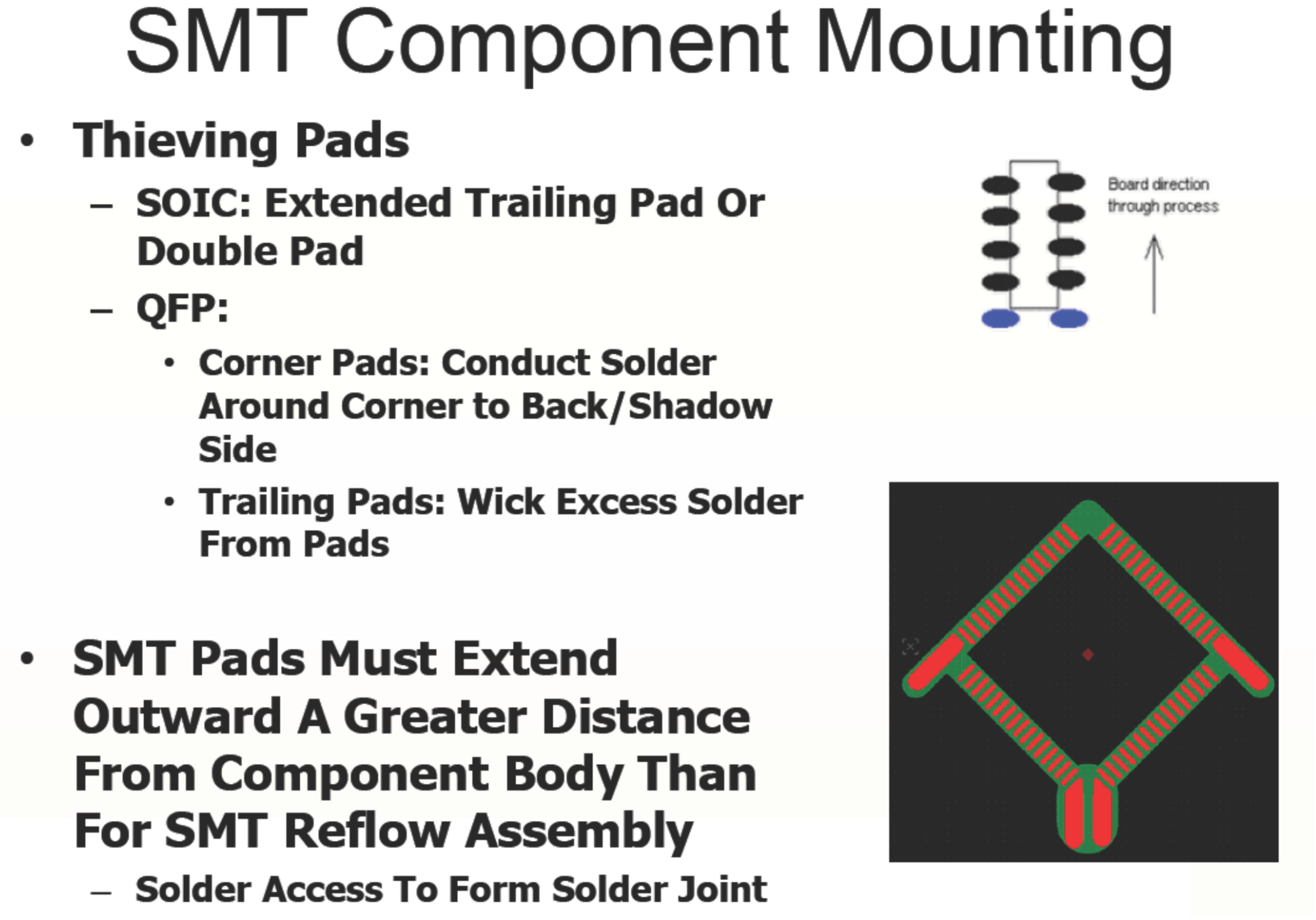
Reference: IPC-SM-782, Section 13.1

Component & Land Dimensions for a DIP

SMT Component Mounting

- **Dual In-line Packages – Leads Pointing At Conveyor**
  - **Passives**
  - **SOT**
  - **SOIC**
- **QFP Oriented At 45 Degrees**
  - **Thieving Pads Required**

Component & Land Dimensions for a DIP



SMT Component Mounting

- Thieving Pads
  - SOIC: Extended Trailing Pad Or Double Pad
  - QFP:
    - Corner Pads: Conduct Solder Around Corner to Back/Shadow Side
    - Trailing Pads: Wick Excess Solder From Pads
- SMT Pads Must Extend Outward A Greater Distance From Component Body Than For SMT Reflow Assembly
  - Solder Access To Form Solder Joint

Component & Land Dimensions for a DIP

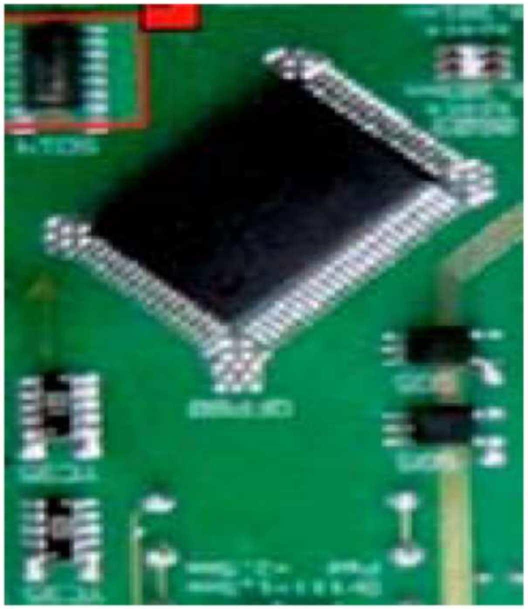
SMT Thieving Pads

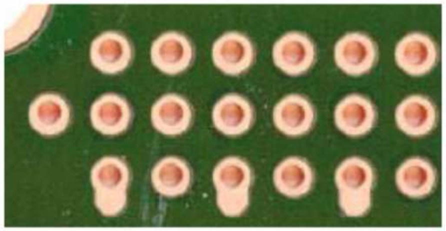
Purpose Is:

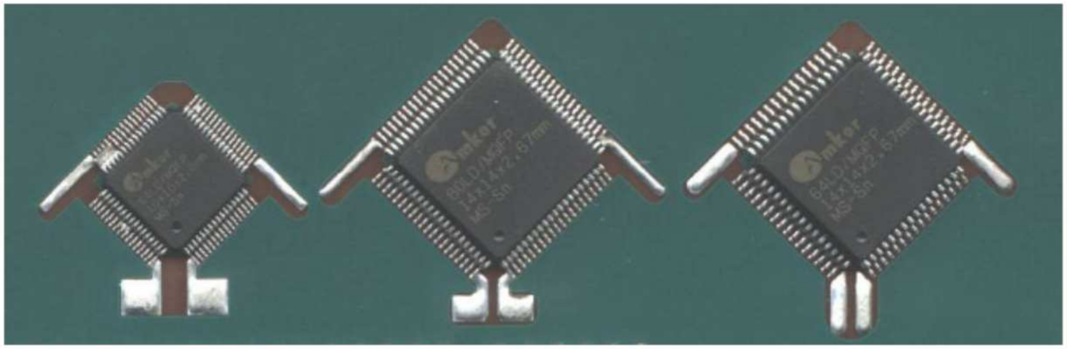
To Wick Excess Solder Away From Pins

Provide Solder Wave Surface Tension Breaking Points

Direct Flow of Solder to Pins and Around Features







Component Spacing

- There is no limit on maximum interpackage spacing

- Land to land spacing between adjacent components should be 1.25 mm clear space all around the edges of the printed board if boards are tested off the connector or 2.5 mm minimum if vacuum seal for testing is used.

Source: IPS-SM-782A, Section 3.6.1.1, pp 20

Component Spacing

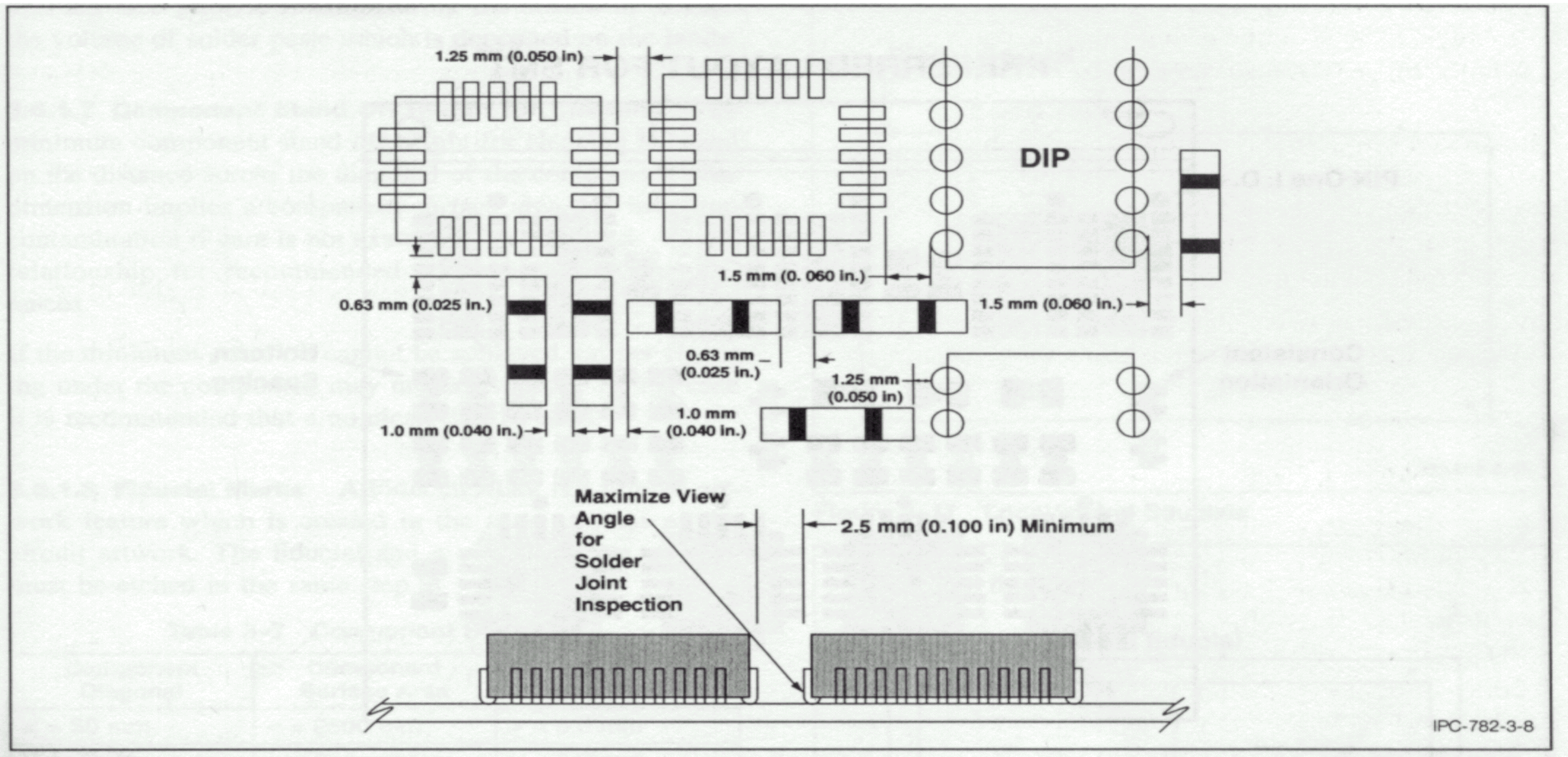
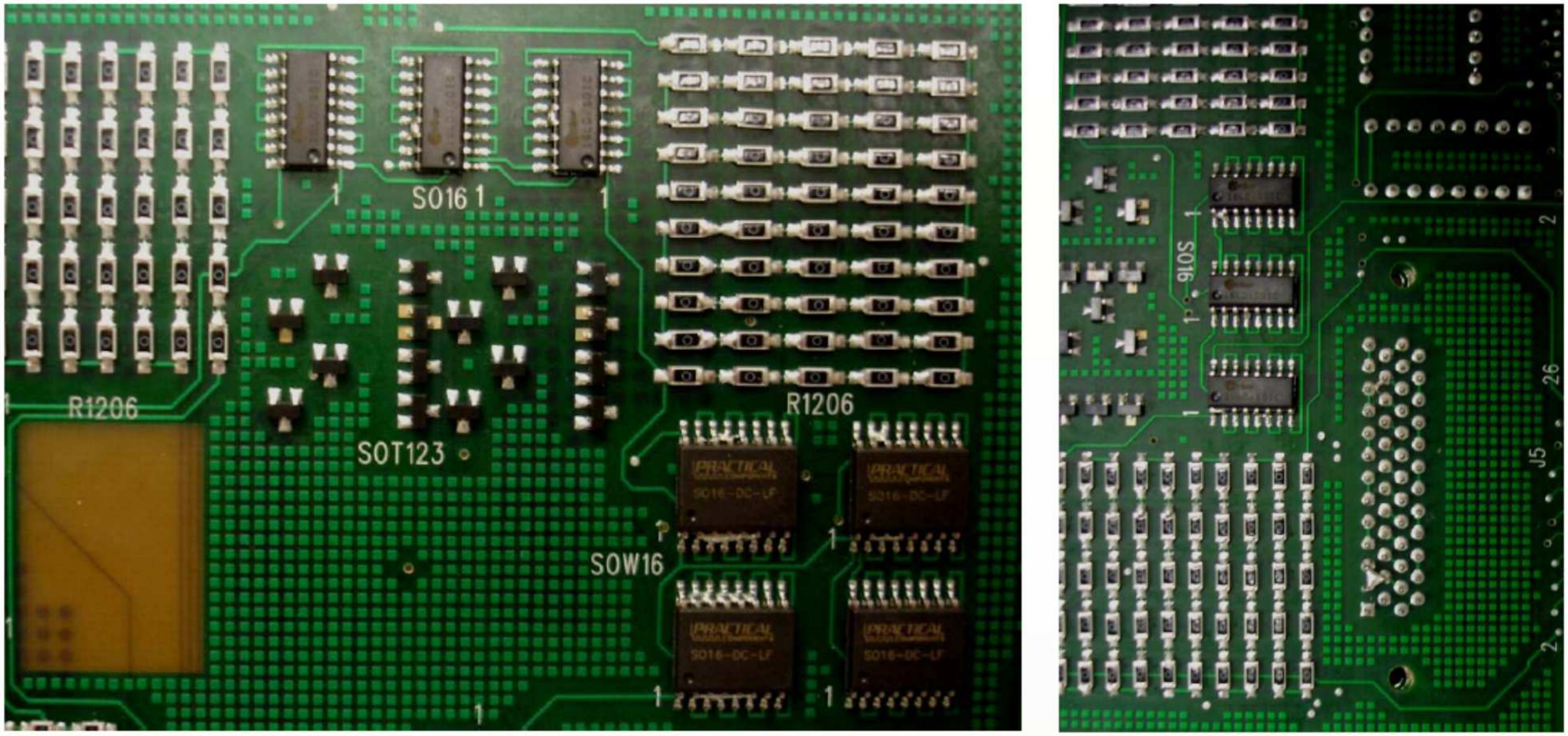


Figure 3–8 Recommended minimum land-to-land clearances

Source: IPC-SM-782A, page 21

PCB Orientation to Wave

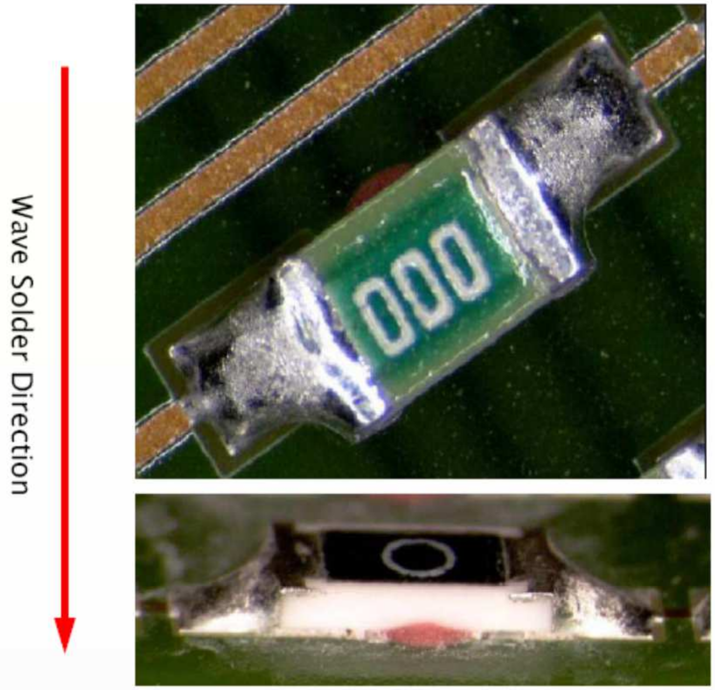
Poor SMT Orientation For Wave



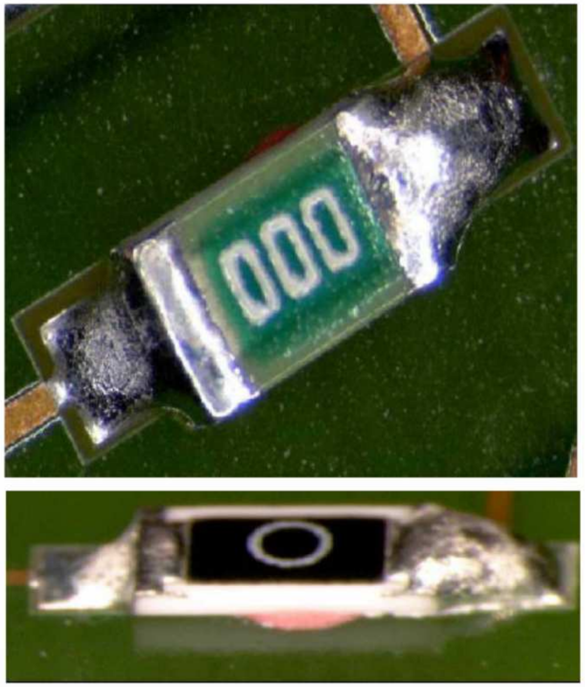
Multiple Solder Skips and Bridges On SMT Components
Bridges on Thru-Hole Components

PCB Orientation to Wave

Chip Pad Design for Wave Soldering



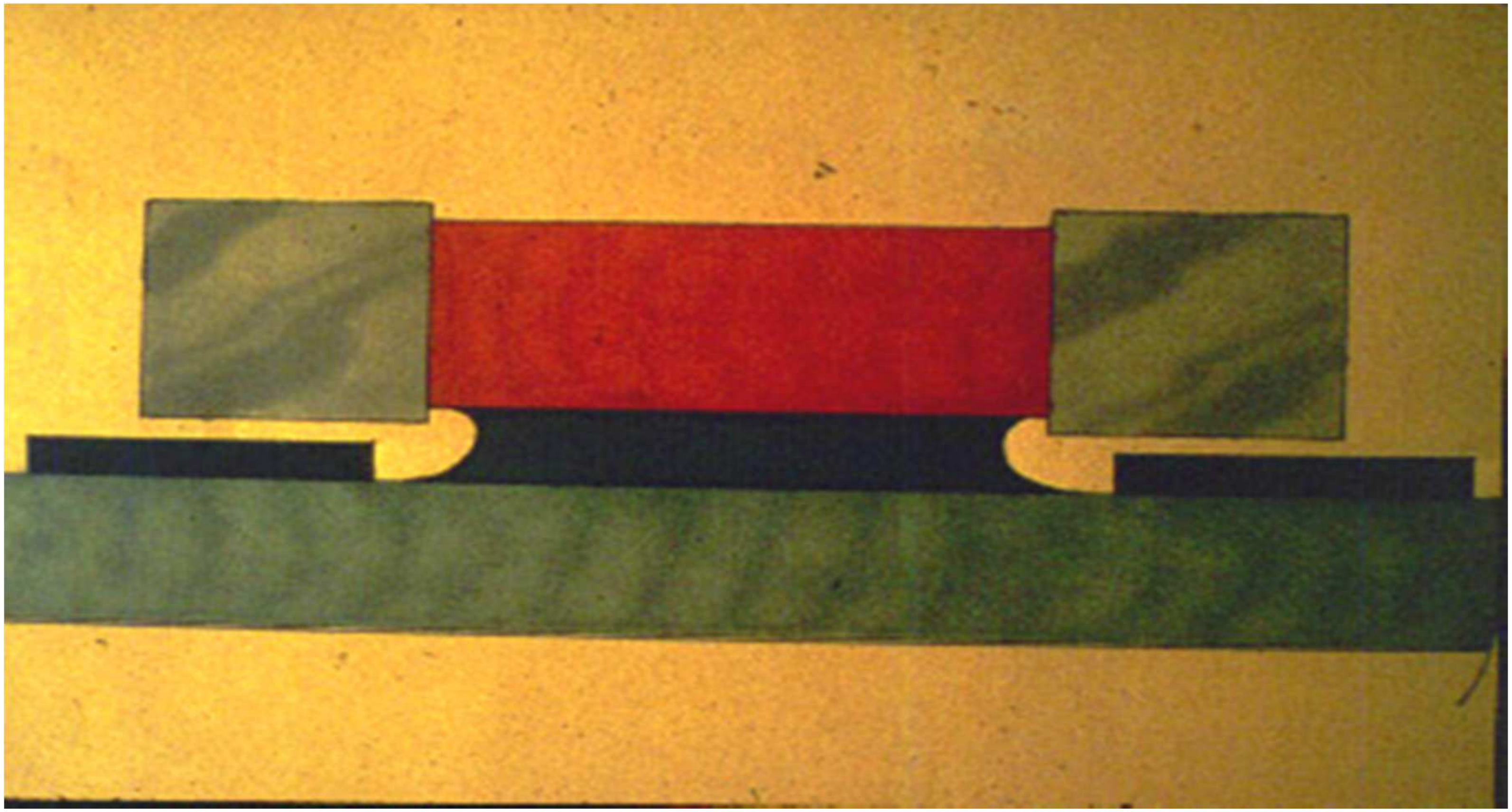
Solder Pads Oriented to Conveyor Rails



Solder Pads Oriented to Solder Pot

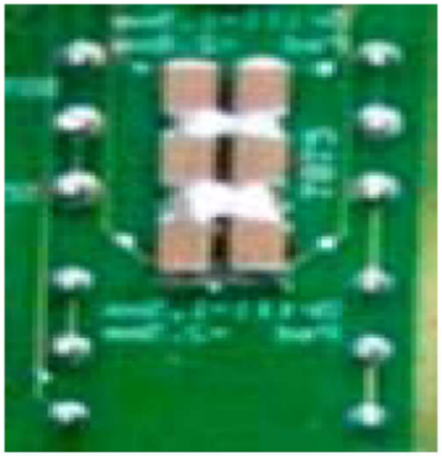
Glue Attachment

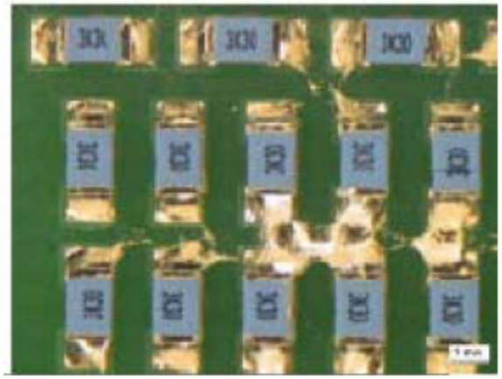
Just strong enough to get through the wave



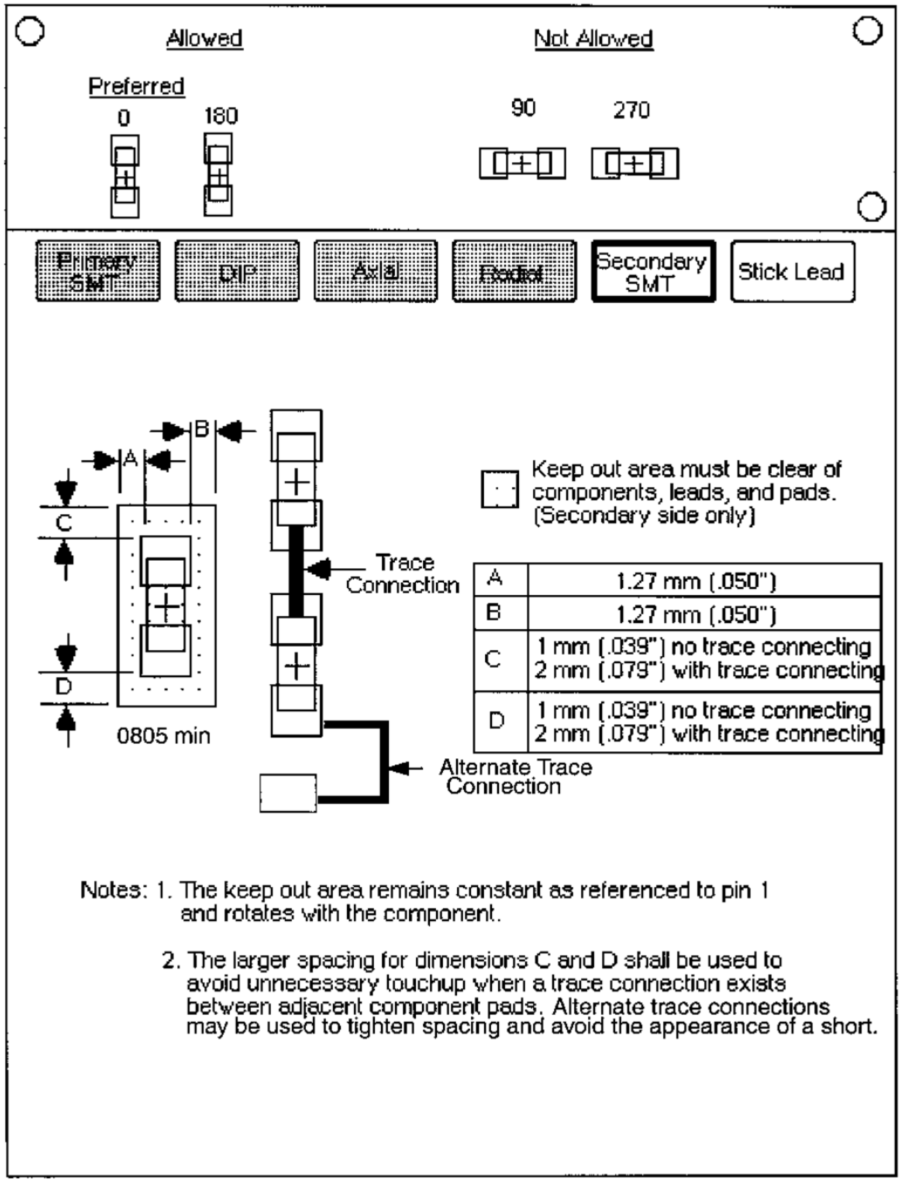
Component Placement Secondary Side

- No SMT Parts Under Solder Tail Parts
- No Passive Packages Smaller Than 0603
- No Passives Packages Greater Than 2025 (Tin/Lead-Only)
  - Lead Free Soldering Maximum Component Size Will Be Smaller
- No SMT QFP Packages less than 0.65mm pitch
- No Large/Tall SMT SOIC Packages
- No Tall Components on Secondary Side (Wave Side)
- Tighter Component Spacing With Nitrogen





SMT Passive Chip Spacing for Wave Solder



Keep out area must be clear of components, leads, and pads. (Secondary side only)

A	1.27 mm (.050")
B	1.27 mm (.050")
C	1 mm (.039") no trace connecting 2 mm (.079") with trace connecting
D	1 mm (.039") no trace connecting 2 mm (.079") with trace connecting

Notes: 1. The keep out area remains constant as referenced to pin 1 and rotates with the component.

2. The larger spacing for dimensions C and D shall be used to avoid unnecessary touchup when a trace connection exists between adjacent component pads. Alternate trace connections may be used to tighten spacing and avoid the appearance of a short.

Component Orientation for Wave Solder Applications

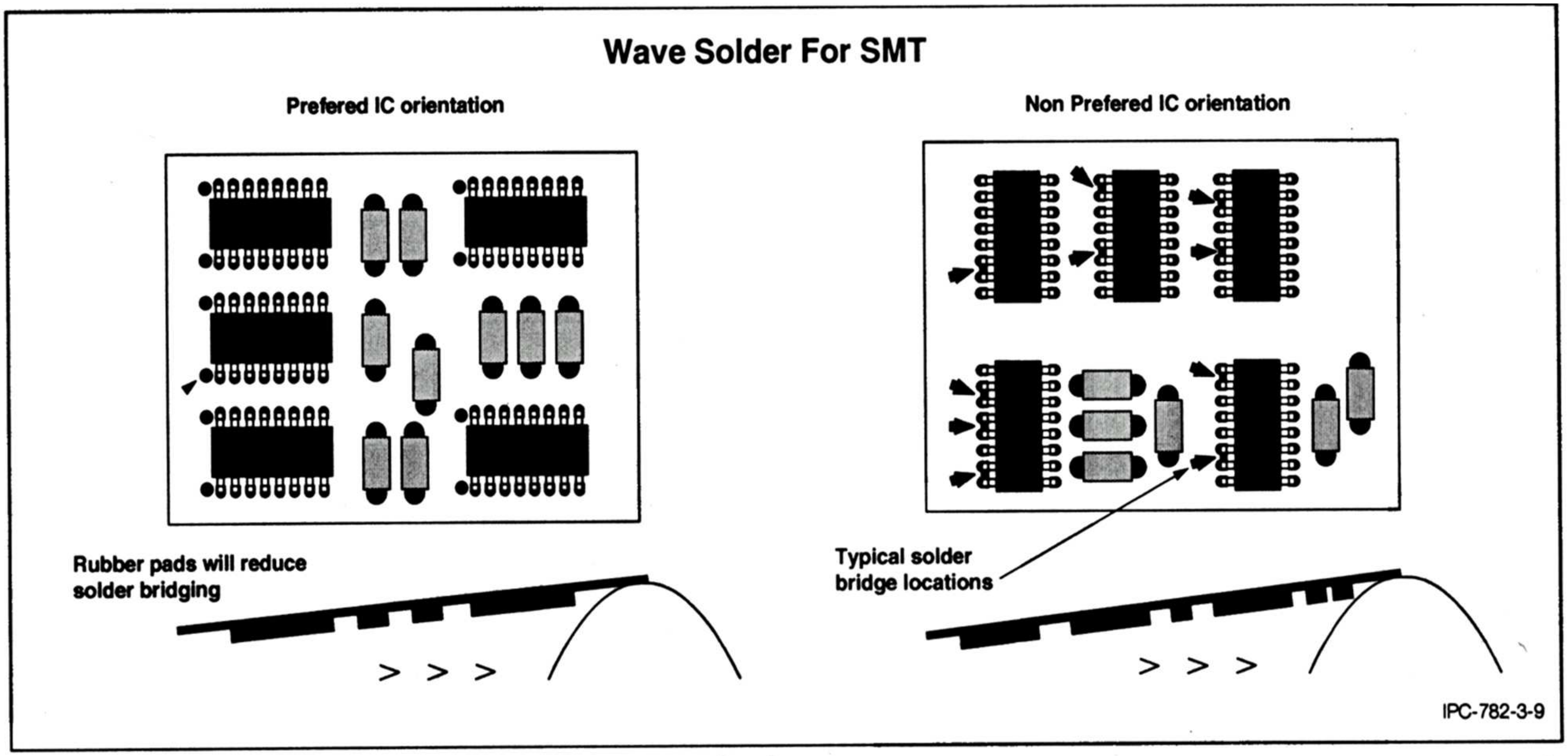


Figure 3–9 Component orientation for wave solder applications

Source: IPC-SM-782A, pp 21

Wave Soldering
Component Orientation

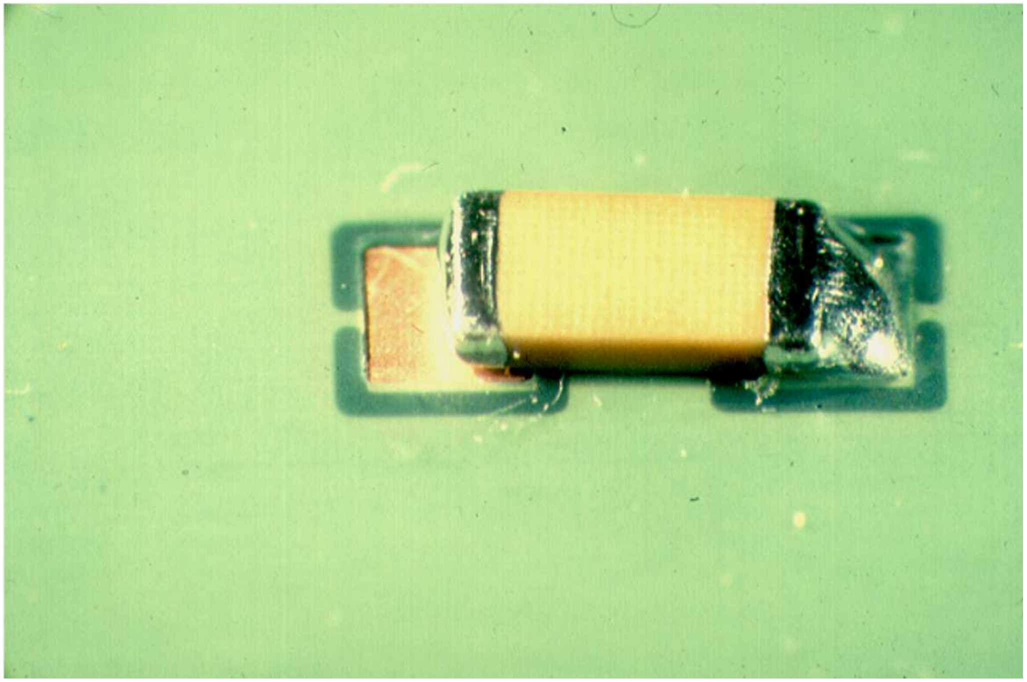
- All passives should be mounted parallel to each other
- All SOICs shall be perpendicular to the long axis of passive components

- The longer axes of SOICs and of passive components should be parallel & perpendicular respectively to the direction of travel of the printed board along the conveyor of the wave soldering machine

Source: IPC-D-330, Section 11, pp 4

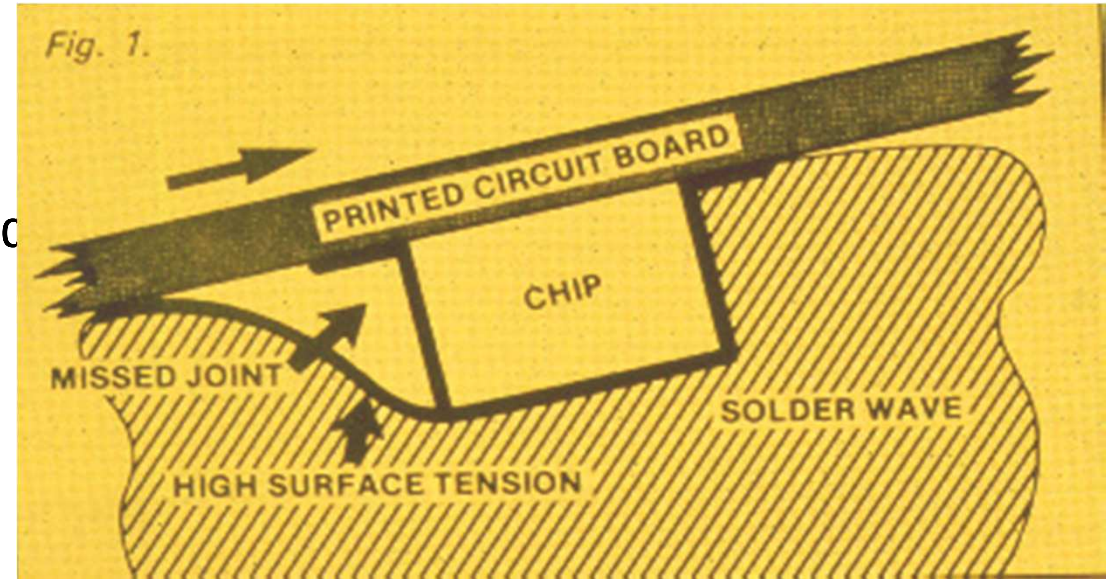
Solder Skips
Some Reasons Why

- Insufficient flux
- Flux not active enough
- Flux over thinned or old
- Solder wave low
- Solder wave not even
- Conveyor speed too fast
- Board warpage
- Hole to lead ratio too large
- Solder mask in hole

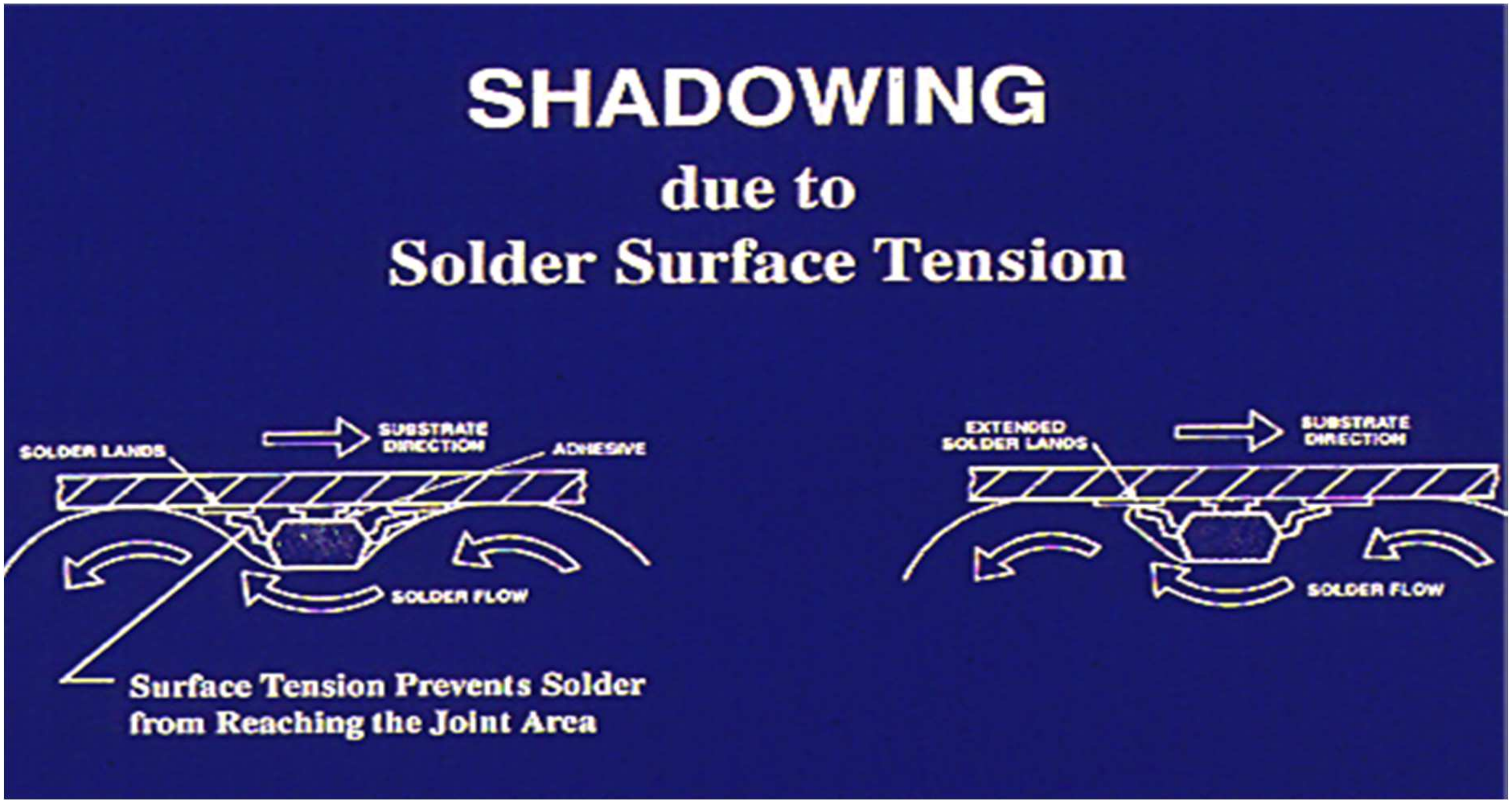


Skips: Possible Causes

- Bent Fingers
- Bent Pallet
- Bent Rails
- Solder Pot not Level
- Bowed boards
- Overshadowing by another lea
- Shadowing
- Poor component orientation
- Clogged chip wave nozzle(s)
- Not using chip wave
- Rotary speed on rotary chip wave too slow



Skips from Shadowing



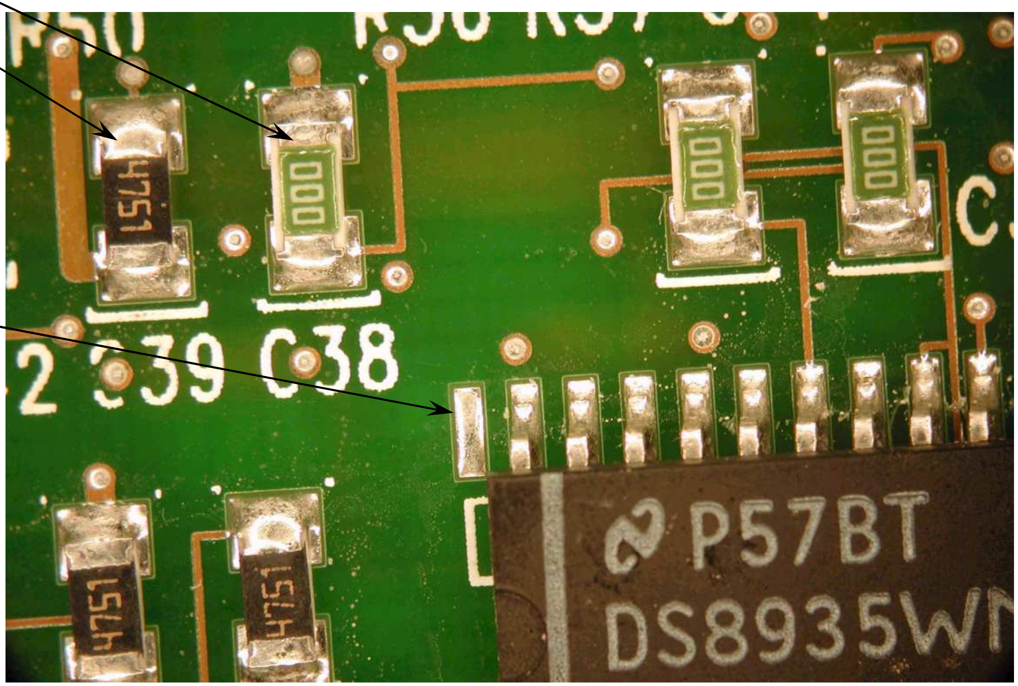
Surface Tension Prevents Solder from Reaching the Joint Area

Component Orientation

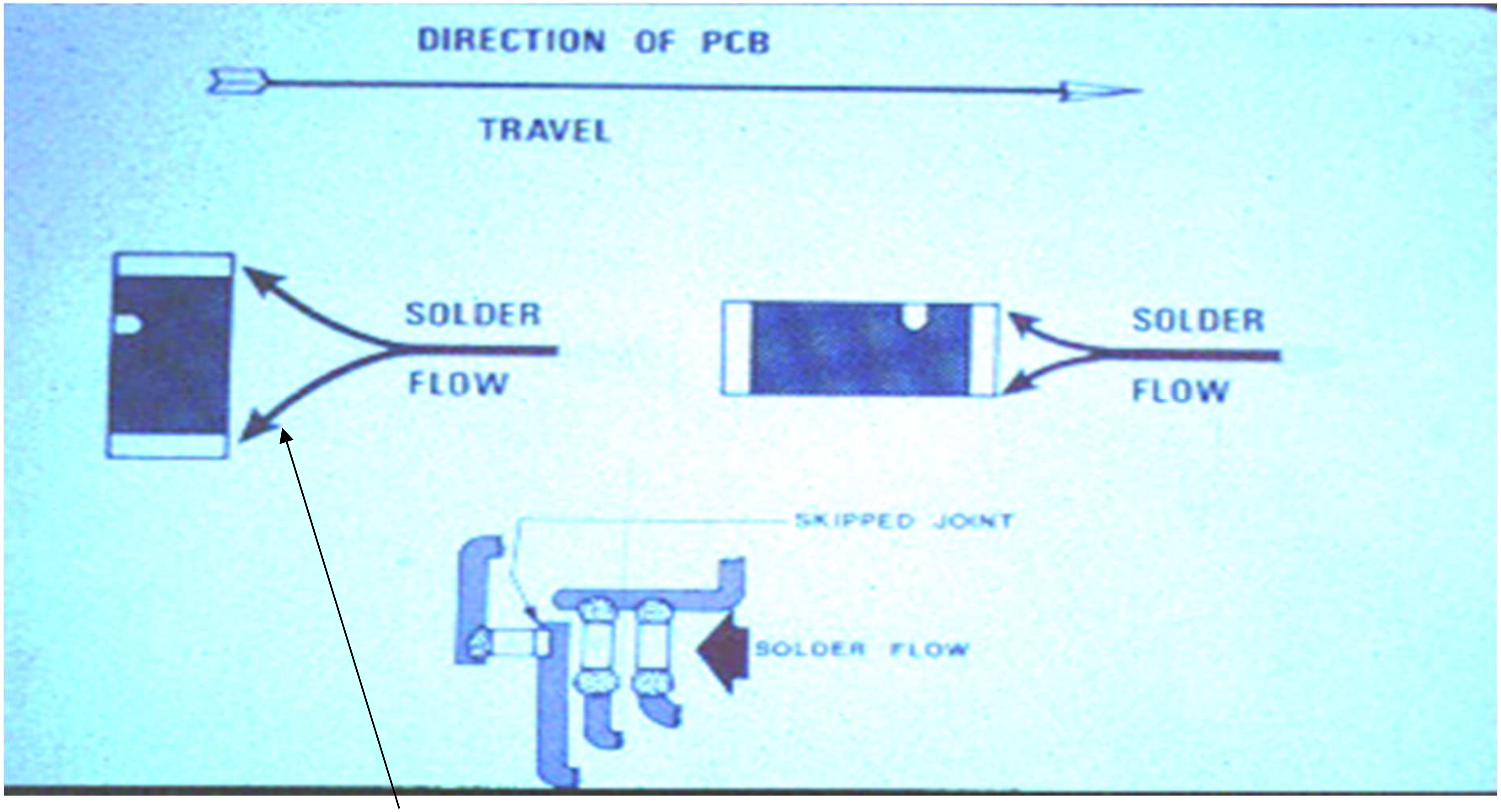
Direction of Travel of Board

Passives Mounted Parallel to each other

Solder Thief to prevent Bridging



Component Orientation



Better

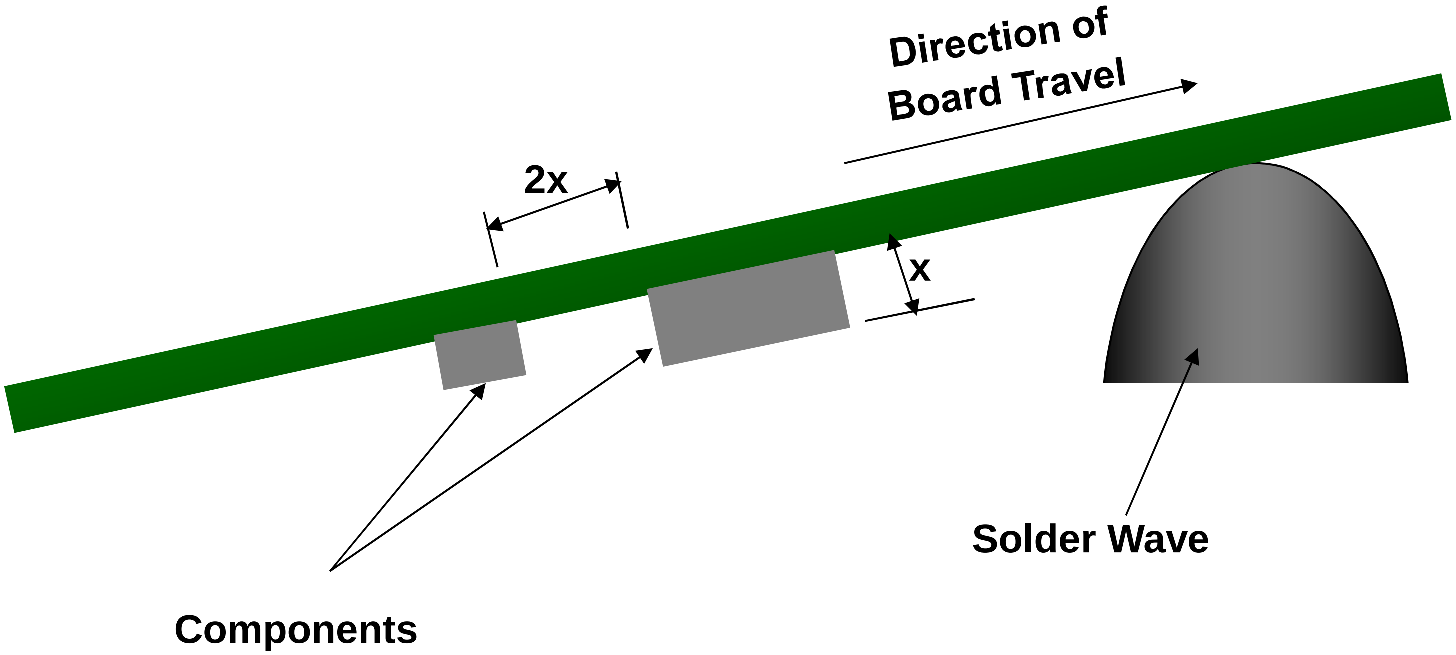
Wave Soldering Component Orientation

- Components should also be placed so that they do not shadow other components

- Components which block access of the wave to the component leads must have spacing distance at least twice the height of the tallest component, this allows the wave to contact any shielded solder joint.

(Reference: Printed Circuits Handbook, pp 5.36, Coombs, ISBN: 0-07-012754-9)

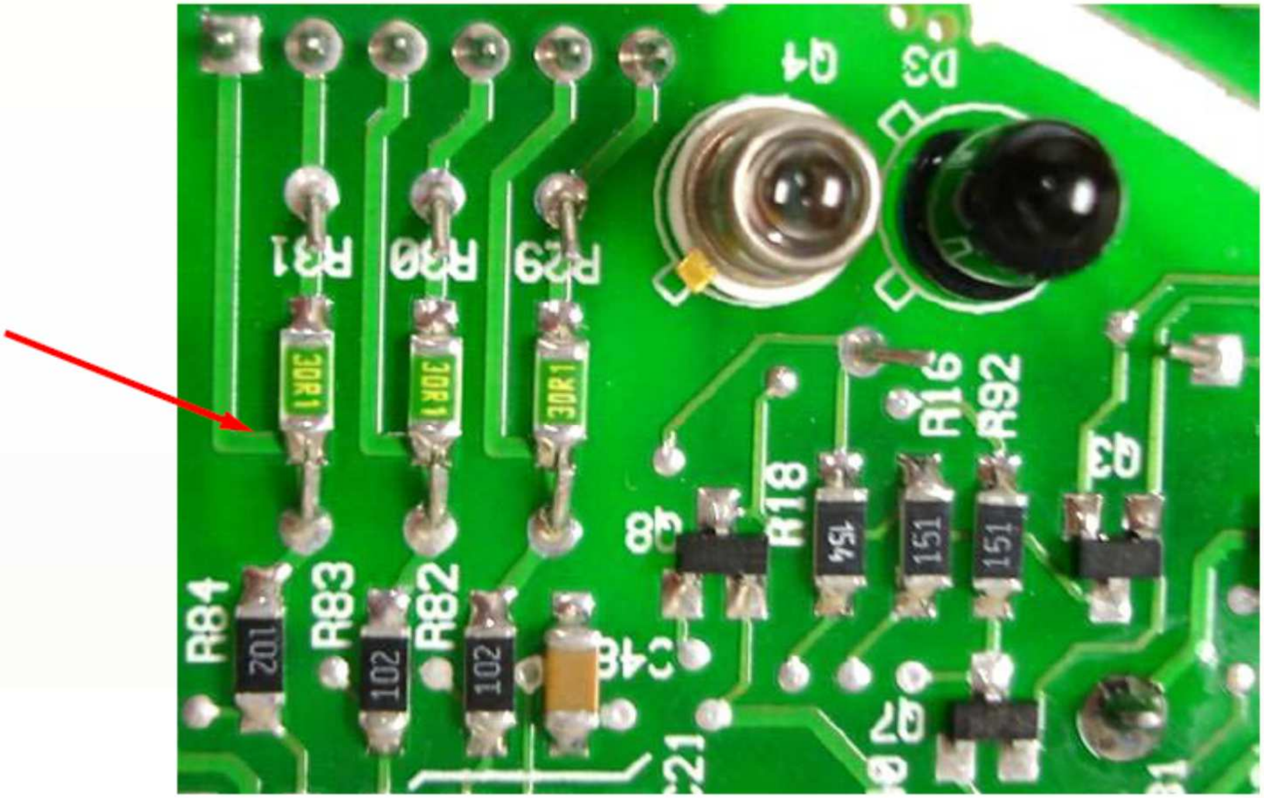
Wave Soldering Component Orientation



Through Hole Component Mounting

Lead Clinching

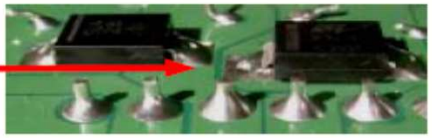
- Away From Components (SMT & Through-hole)
- Away From Exposed PCB Conductive Feature (Via, Trace)



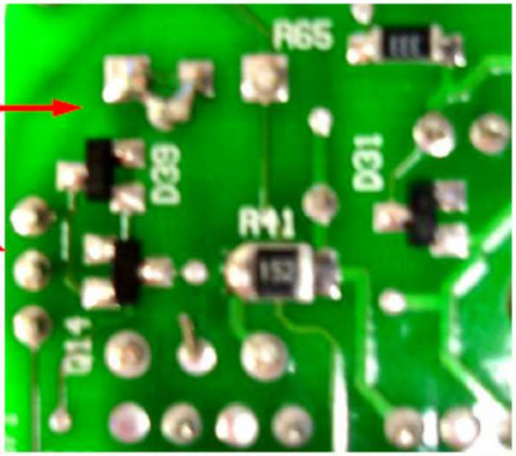
Through Hole Component Mounting

Lead Length

- Leads Should Extend Below Bottom of Board

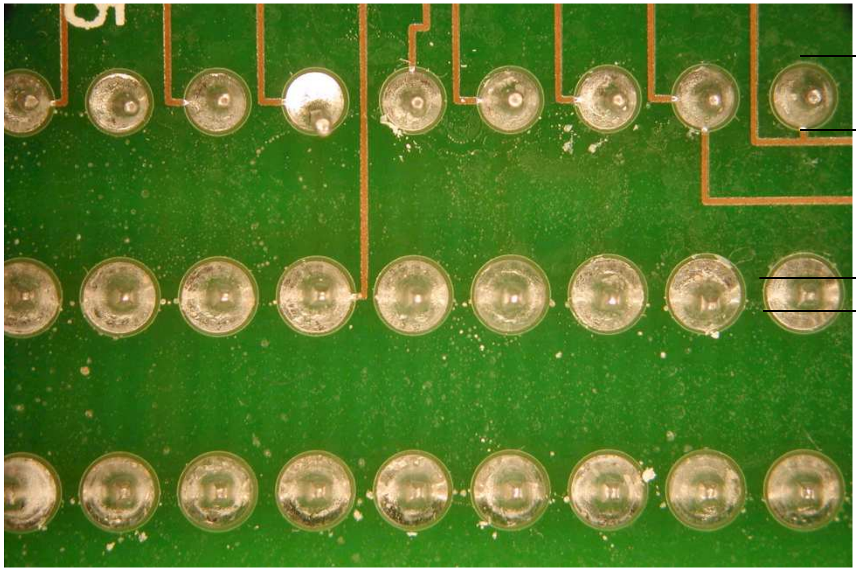


- Lead Protrusion: Shorter is Better
  - Decreased Solder Bridging
  - Decreased Component Tilting



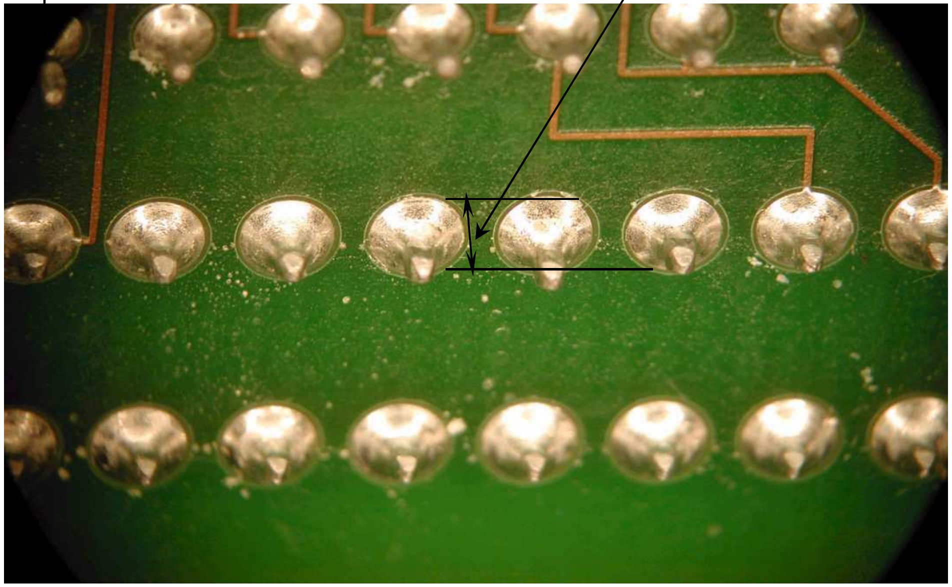
- Lead Free Solder:
  - Lead Length Should Be Even Shorter Than Tin-Lead Solder.

Lead Protrusions



Pad Diameter

Pin Diameter



Lead Height

$$\frac{\text{Lead Height}}{\text{Pad Diameter}} = 1.1 \text{ or } 1.2$$

Pad Diameter = 3 x pin diameter, but at least 0.025 inches

Lead Protrusions

- For single sided PCB Assembly, lead or wire protrusion must be a minimum of 0.5 mm for all classes

- For double-sided and multilayer PCB Assembly, in all classes, the minimum lead protrusion is that the lead end be visible in the solder

- The maximum lead protrusion for Class 1 is that there should be no danger of shorts

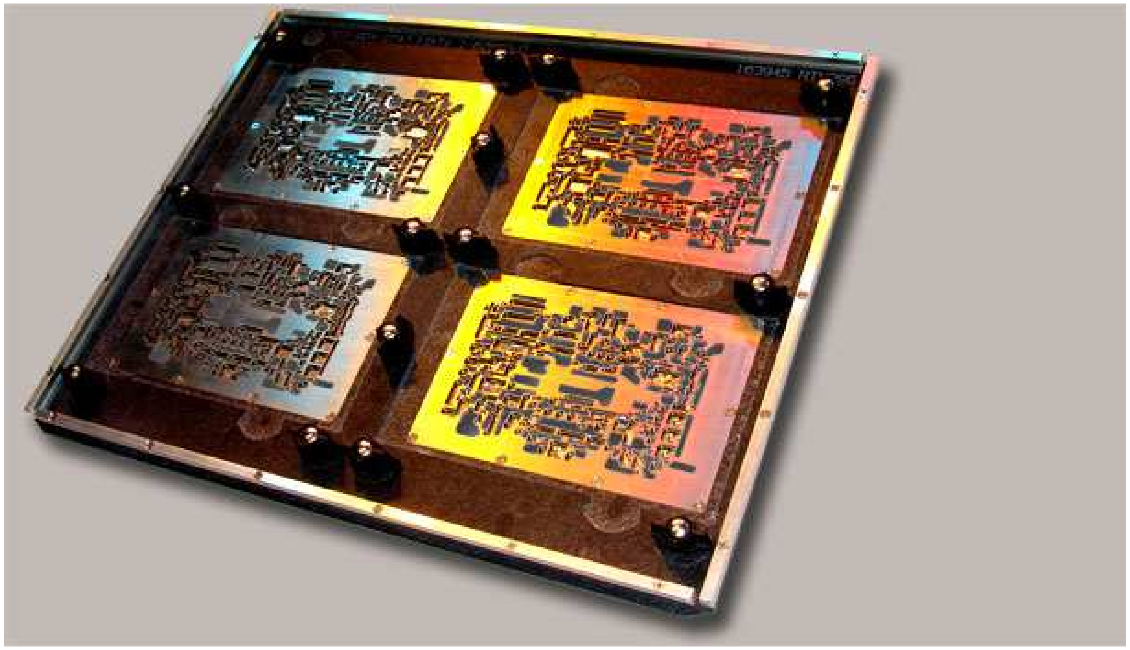
Lead Protrusions

- For Class 2, the maximum lead protrusion is 2.5 mm and for Class 3 the maximum lead protrusion is 1.5 mm

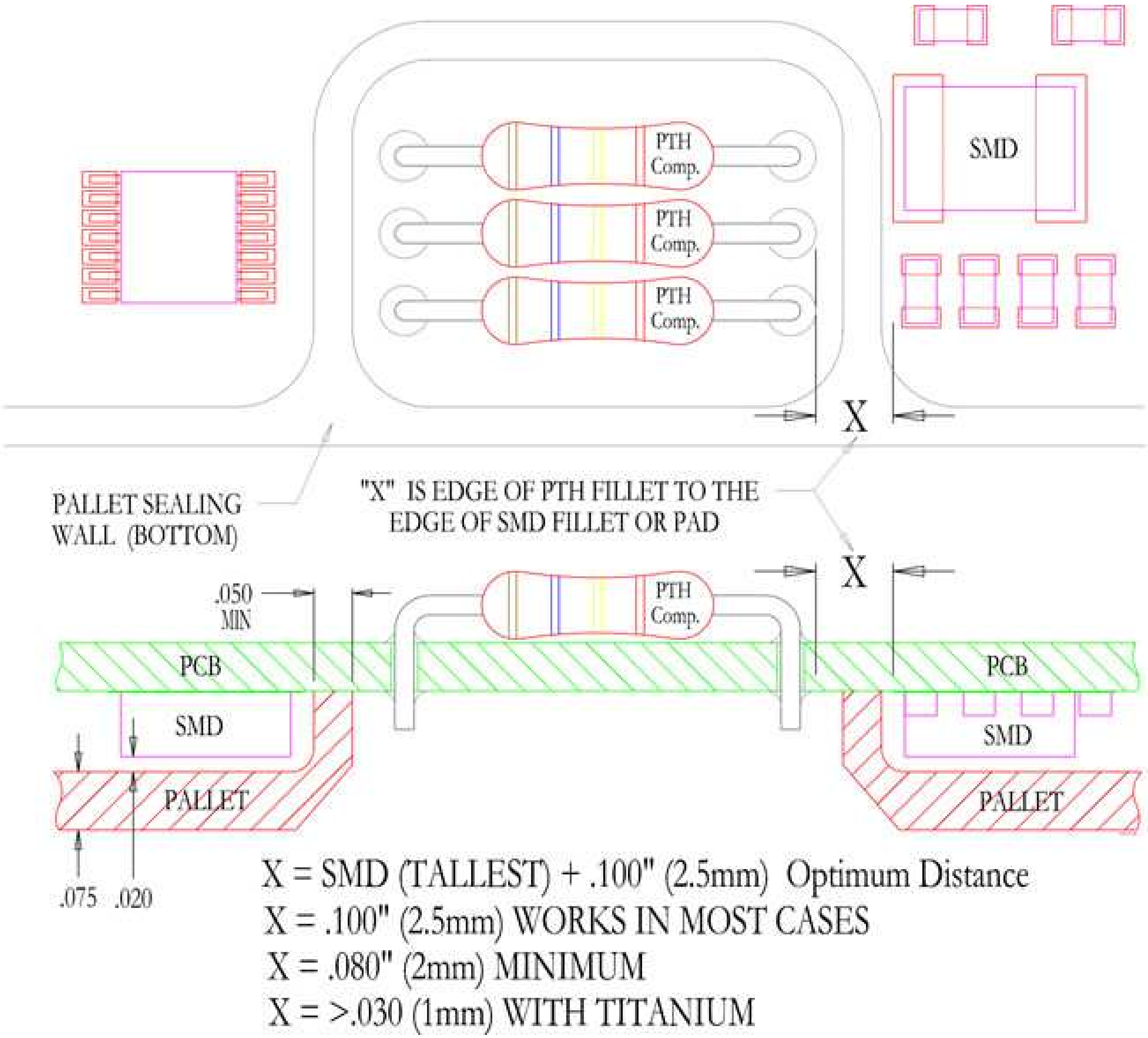
- For boards thicker than 2.3 mm, the lead protrusions may not be visible

Source: Printed Circuits Handbook, pp 36.27

Wave Solder Pallets



Wave Solder Pallets



X = SMD (TALLEST) + .100" (2.5mm) Optimum Distance
X = .100" (2.5mm) WORKS IN MOST CASES
X = .080" (2mm) MINIMUM
X = >.030 (1mm) WITH TITANIUM

Software Tools Developed by Doctor Ron Lasky

Ronald C. Lasky, Ph.D., PE
Instructional Professor, Thayer School of Engineering,
Dartmouth College
Director, Cook Engineering Design Center
Director, Lean Six Sigma
Lean Six Sigma Master Black Belt Instructor
Senior Technologist, Indium Corporation
8000 Cummings Hall, Dartmouth College
Hanover, NH 03755

LineSimulator™

- A tool that aids in attaining the most effective use of inventory, capital equipment, time, and manpower is LineSimulator™. LineSimulator is an Excel®- based software tool which aids in the design and optimization of SMT assembly lines for maximum productivity. LineSimulator enables line simulation to be performed easily, and at a low cost, as it offers most of the operations of expensive software such as Arena®- and Witness®-.
- While LineSimulator offers a low-cost alternative to expensive productivity software, many feel that it's ease of use and intuitive simplicity are it's biggest assets.

ProfitPro™ (cost)

REAL-TIME COST ESTIMATING

- Real-time cost estimating simply uses the elements of cost as discussed in the introduction and calculates the cost and number of boards produced. While it is simple in concept and involves no sophisticated mathematics, the calculations are quite tedious and cumbersome as they include many production variables such as cycle time, hours per shift, shifts per day, days per week, set up time, unscheduled and scheduled downtime. Yield loss and cost of repair must be considered as well as inventory turns and interest rates. The equations have been entered into an Excel®-based computer program called ProfitPro™.

ReflowCoach™

- It is well understood that proper reflow is critical to the optimization of an SMT production line. In fact, a proper reflow procedure delivers reduced defects in component attachment, inspection, and in the ultimate solder assembly. Many people struggle with proper reflow design and profiling. ReflowCoach™ is designed to provide information, guidance, and profiling details.
- ReflowCoach™ is an Excel-based software tool for optimizing the reflow process. It combines your reflow furnace's capabilities with your solder materials' recommended procedures to deliver an optimized reflow profile for the assembly you are making. The solder paste specifications are "hardwired" in.

WaveCoach™

- Wave Soldering is among the oldest electronics assembly procedures in practice today. Even with all our experience, we find that improvements can still be gained through the implementation of experience and technology. WaveCoach™, is a tool that may help you improve your Wave Soldering quality, yields, and profitability.
- WaveCoach™ is an Excel-based software tool for optimizing the wave soldering process. It assists in the development and creation of the pre-heat profile and wave soldering machine parameters desired for each specific assembly.

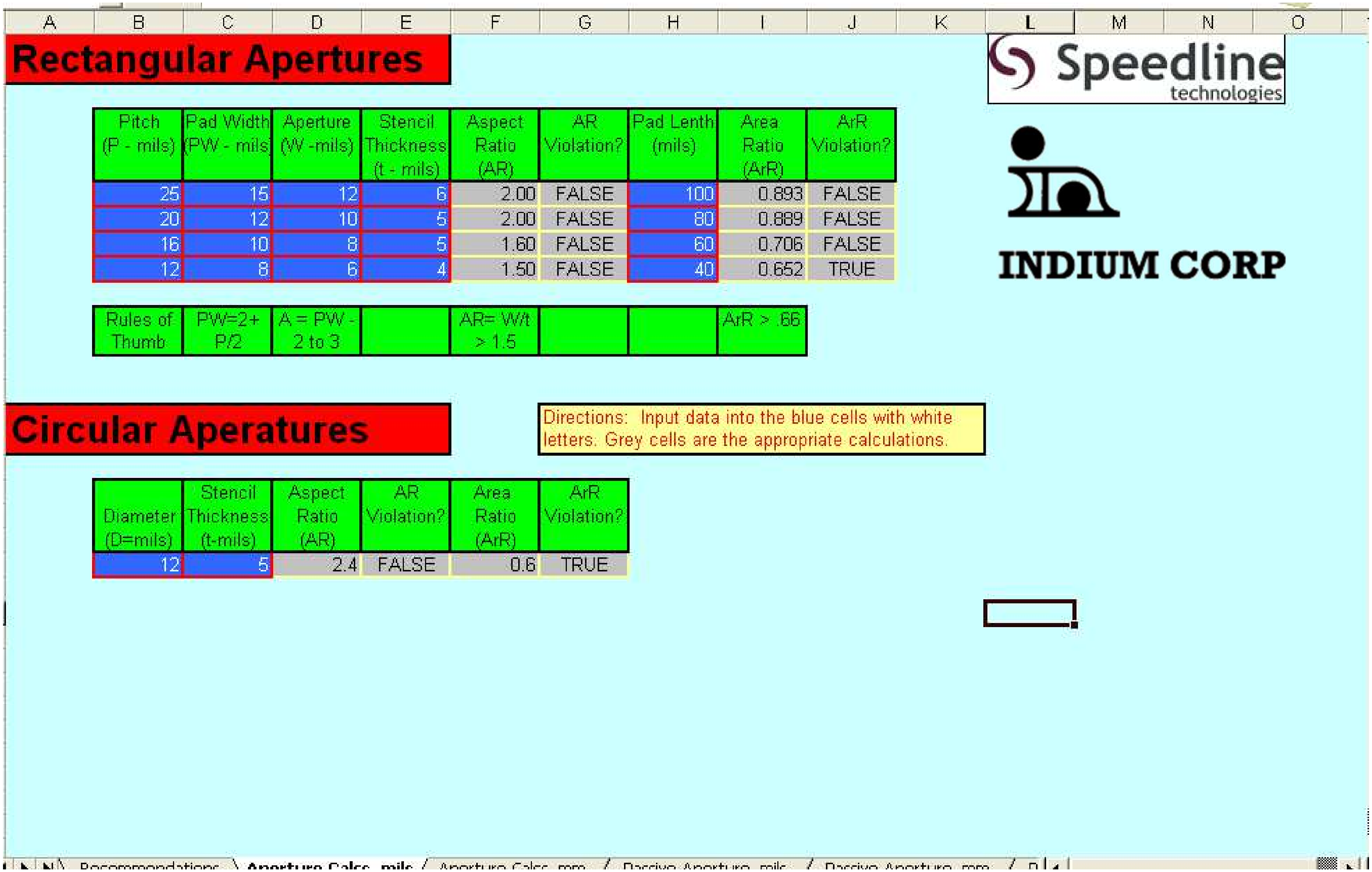
To implement WaveCoach™, you will require:

- A PC with a running version of Microsoft Excel®
- The pre-heat profile
- The specs for the flux you are using in your process
- Wave machine info (conveyor speed & wave length)

StencilCoach™

- Can be used to calculate stencil aperture volume requirement for the Pin in Paste process
- Can be used for all stencil aperture design calculations
- If you would like the software, please e mail me or give me your business card and I will e mail it to you

Stencil Design Software “Stencil Coach” Created by Doctor Ron Lasky



Rectangular Apertures

Pitch (P - mils)	Pad Width (PW - mils)	Aperture (W -mils)	Stencil Thickness (t - mils)	Aspect Ratio (AR)	AR Violation?	Pad Lenth (mils)	Area Ratio (ArR)	ArR Violation?
25	15	12	6	2.00	FALSE	100	0.893	FALSE
20	12	10	5	2.00	FALSE	80	0.889	FALSE
16	10	8	5	1.60	FALSE	60	0.706	FALSE
12	8	6	4	1.50	FALSE	40	0.652	TRUE

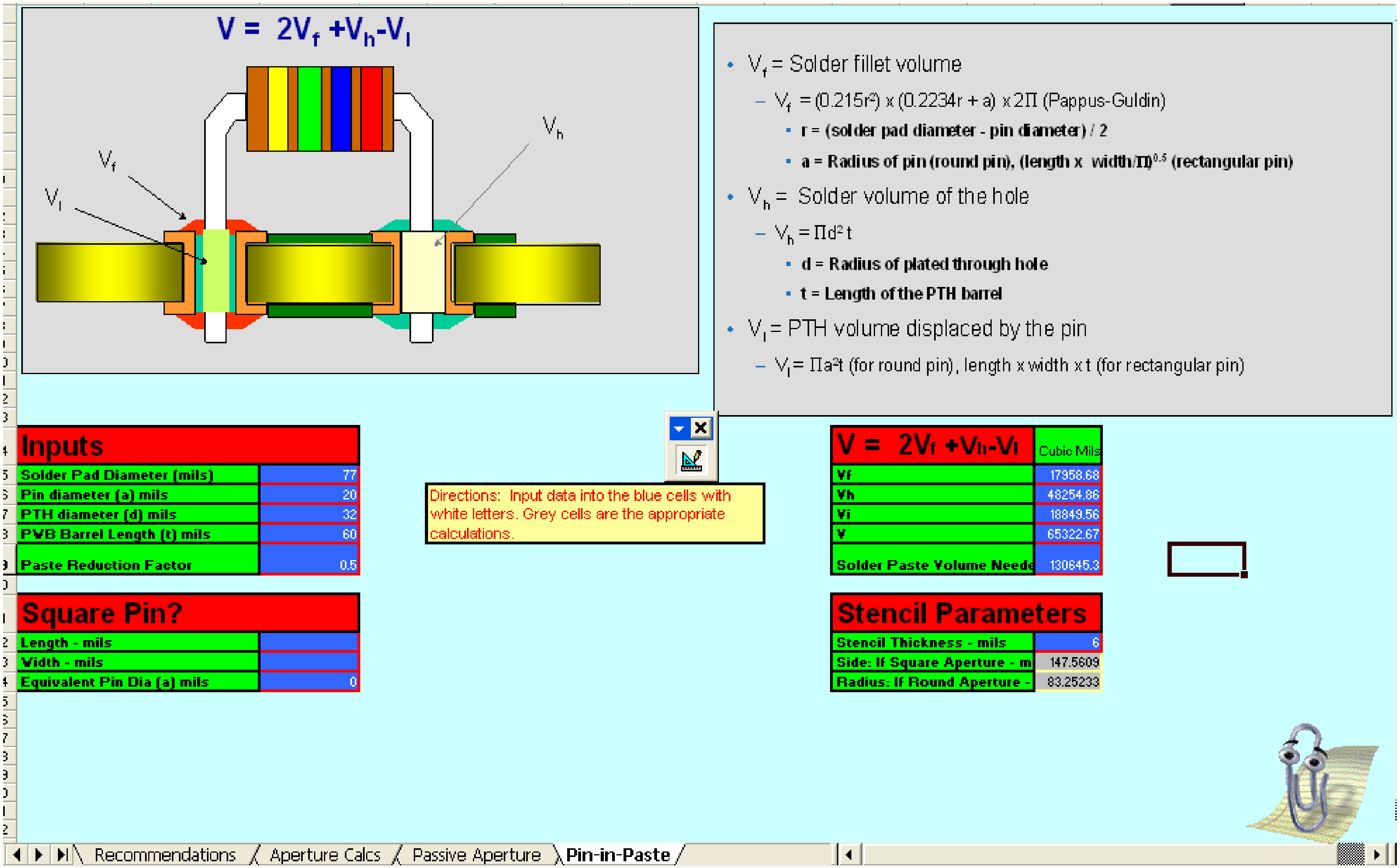
Rules of Thumb	PW=2+ P/2	A = PW - 2 to 3		AR= W/t > 1.5			ArR > .66

Circular Aperatures

Directions: Input data into the blue cells with white letters. Grey cells are the appropriate calculations.

Diameter (D=mils)	Stencil Thickness (t-mils)	Aspect Ratio (AR)	AR Violation?	Area Ratio (ArR)	ArR Violation?
12	5	2.4	FALSE	0.6	TRUE

StencilCoach™



$$V = 2V_f + V_h - V_l$$

- V_f = Solder fillet volume
  - $V_f = (0.215r^2) \times (0.2234r + a) \times 2\Pi$ (Pappus-Guldin)
    - **r = (solder pad diameter - pin diameter) / 2**
    - **a = Radius of pin (round pin), (length x width/Π)$^{0.5}$ (rectangular pin)**
- V_h = Solder volume of the hole
  - $V_h = \Pi d^2 t$
    - **d = Radius of plated through hole**
    - **t = Length of the PTH barrel**
- V_l = PTH volume displaced by the pin
  - $V_l = \Pi a^2 t$ (for round pin), length x width x t (for rectangular pin)

Inputs	
Solder Pad Diameter (mils)	77
Pin diameter (a) mils	20
PTH diameter (d) mils	32
PWB Barrel Length (t) mils	60
Paste Reduction Factor	0.5

Square Pin?	
Length - mils	
Width - mils	
Equivalent Pin Dia (a) mils	0

Directions: Input data into the blue cells with white letters. Grey cells are the appropriate calculations.

$V = 2V_f + V_h - V_l$	Cubic Mils
Vf	17958.68
Vh	48254.86
Vi	18849.56
V	65322.67
Solder Paste Volume Neede	130645.3

Stencil Parameters	
Stencil Thickness - mils	6
Side: If Square Aperture - m	147.5609
Radius: If Round Aperture -	83.25233

“If we did all the things we are capable of, we would literally astound ourselves”

-- Thomas Edison

Thank You!!!!

Joe Belmonte

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